Planned: EMI, current loops, fields

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HELMHOLTZ ASSOCIATION

DESY

Main aspects

- **Minimize the current in common GND paths**
- **Minimizing the dependence on currents of individual blocks, instruments and system**
- **Providing a good current guide for user-currents and induced currents**

- **Direct RF-field has to be taken into account**
  but far field coupling is low at large distances, if the designs are OK.
  Dipole near field decreases with d/r^3
  near field coupling is a issue in compact electronic design

Nothing will get perfect for EMI:

- Not all techniques might be applicable to all stages:
  Block, PCB, instrument, rack, system
- Not optimizing a step requests higher effort at other stages.
- Late in the development optimizing is often hard to do or impossible.

⇒ **Where possible plan it in the beginning**

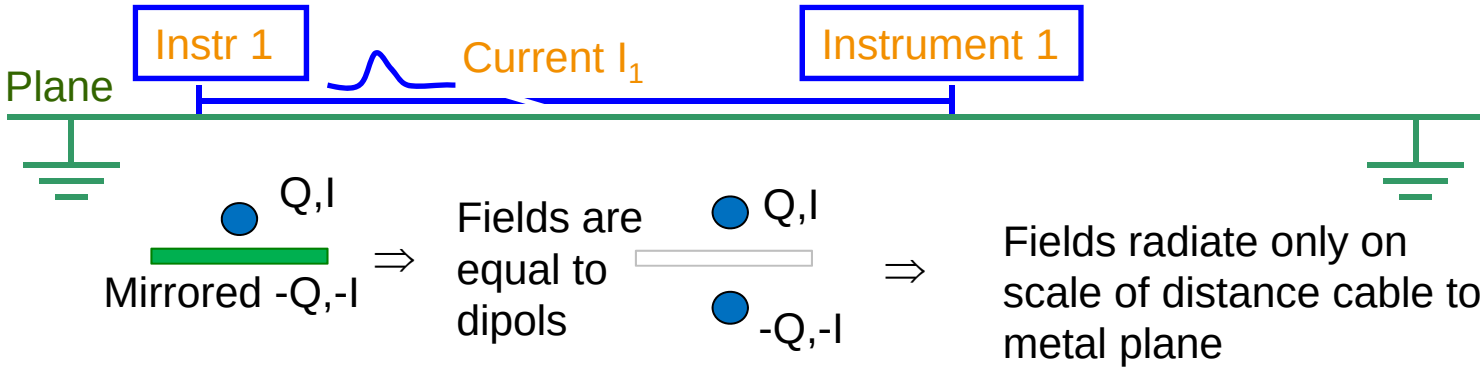
The presentation is the EMI-view and not already practical compromises

Outline

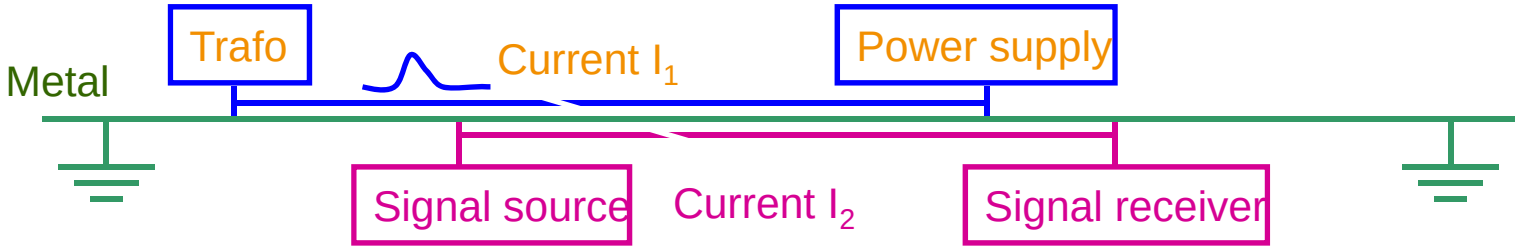
- Reminder: Coupling mechanisms
- Basic idea of the goal “GND planning”
- Methods to Identify critical paths
- Issues for PCB design
- Decoupling for system design

General: EMI couplings

➢ Fields radiation



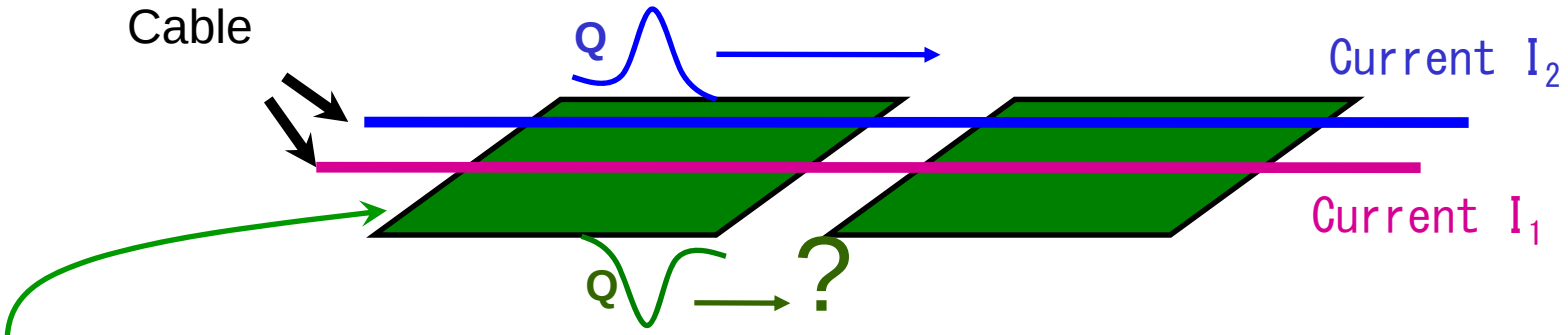
➢ Conductor ... Experience : Most remaining disturbances happen here



Need careful planning at

- signal types, transfer, mechanics, instrument selection

2. Coupling mechanisms: Capacitive

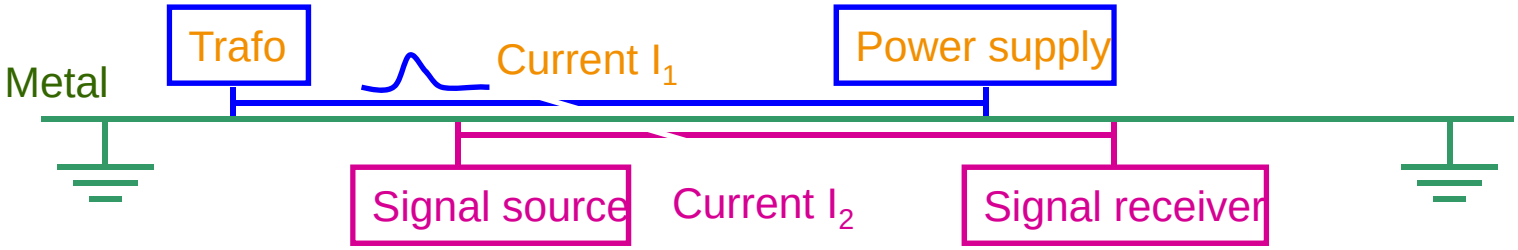


- Cable with non-compensated (not completely) voltage-signal
  C/length=$\varepsilon_0\pi$/ln(distance/radius) = 12pF/m
  distance=5mm, radius=0.5mm
- Routed on metal support ➡ Mirrored current on support
- At interruption of support: What can happen?

  Large way around; Use other cable (=noise, crosstalk)

⇨ Voltage-compensation on small distance: U_2=-U_1(AC), I_2=-I_1
⇨ Interconnections at small distances (grid) in the ground
⇨ Small distances of signal cables to metal support

3. Coupling mechanisms: Impedance



e.g. Ground is used for

- Reference
- Current return
- Safety ⇐ Must, don't disconnect

Need

- Planning, how it is used where
- Impedances where

Making the construction independent of currents in the GND system
EMI-zoning Main conceptional system issue!!!!

Goal: minimize the coupling between different areas or functions

- Minimize Z_K
- Maximize Z_E

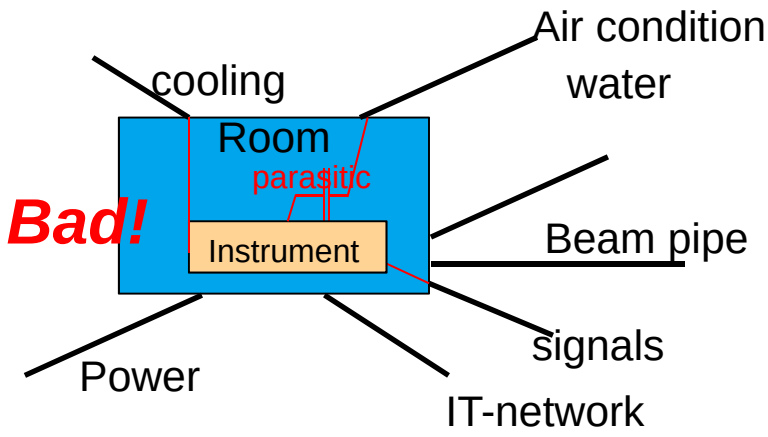
Minimize Z_K: Plan all metal connections

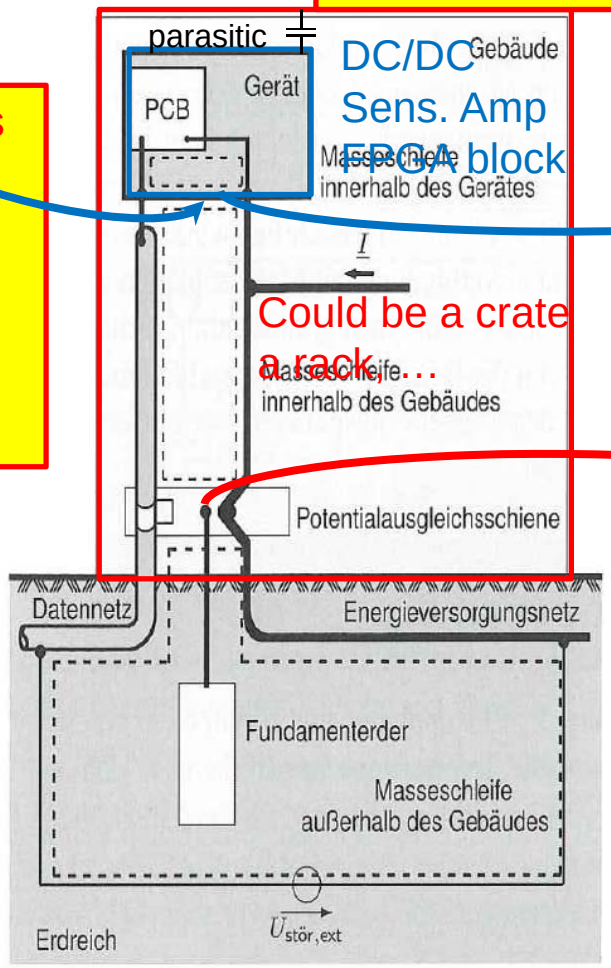
- All connections at ONE point to a zone: block, PCB, chassis, rack
- Afterwards/before distances of conductors to limit crosstalk: "Loops"

Maximize Z_E

- Hard to get low Z_K? than apply filters

Multiple zoning: "parasitic coupling" The hutch can already be a good shielding, if free of current





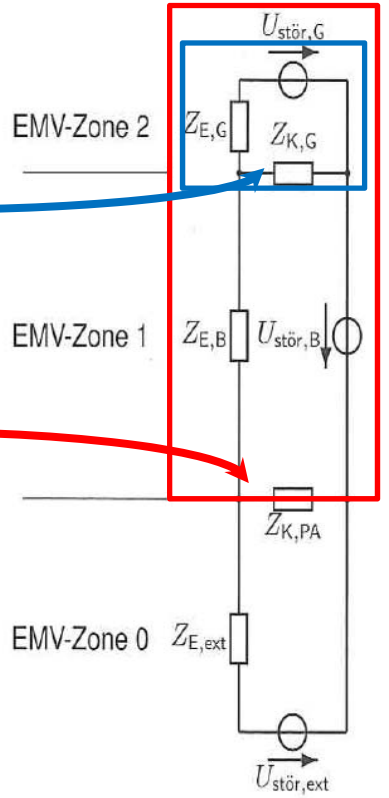


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Bild 7.32: Masseschleifen in einer Anlage und ESB

Example: Planning GND-currents in a Crate, PC, …. Z_K

Aim: Small coupling Z_K

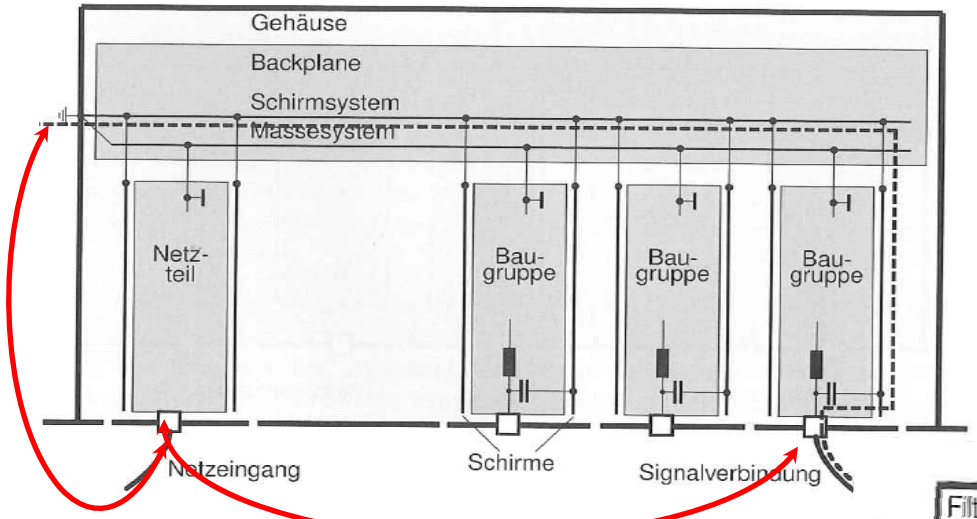
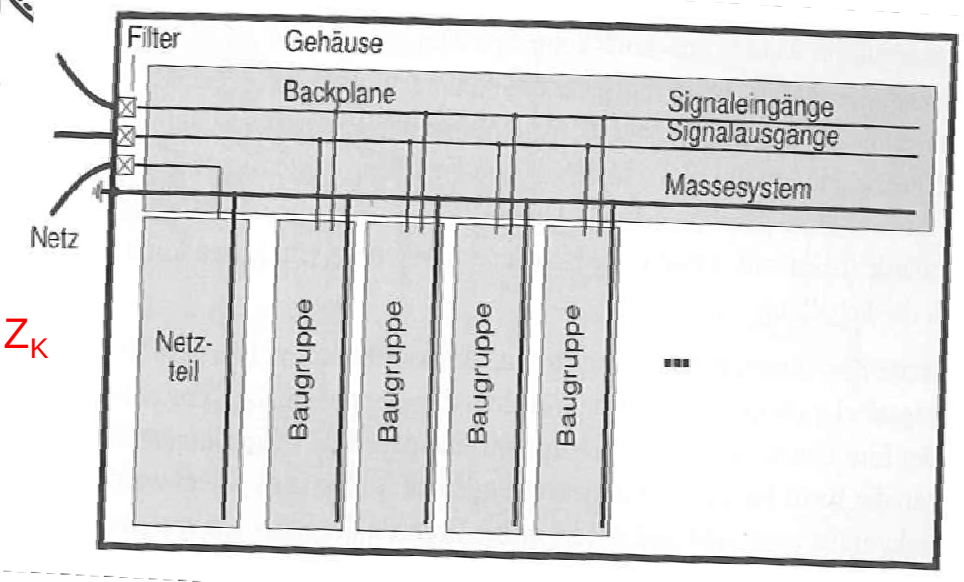


Bild 8.23: Falsch geplante Struktur eines Baugruppenträgers

Bad: Large couplings Z_K

Multiple zonings:
- Chassis
- Each group



Small Z_K

Remark:
- Far ends of groups are free antennas for E-Field … see later

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Example: Planning the couplings in a PCB …. $>Z_E$

Aim: Large: coupling Z_E

Planning two zones

(Each closing their own currents
otherwise the large GND-connection
might cause problems. Smaller coupling
might be larger antenna)

Zones can be:

- e.g. High frequency part e.g. FPGA
- Sensitive part
  analogue-in to ADC
  (functional zoning is not mechanical zoning:
  A function can be on RTM+AMC)

High Z_E can be reached by

- Differential signals: Transformer, LVDS, analogue differential
- Common mode still present due to parasitic: R,Ferrites
- Limiting rise times: R in SPI, I^2C-device provide minimal rise time.

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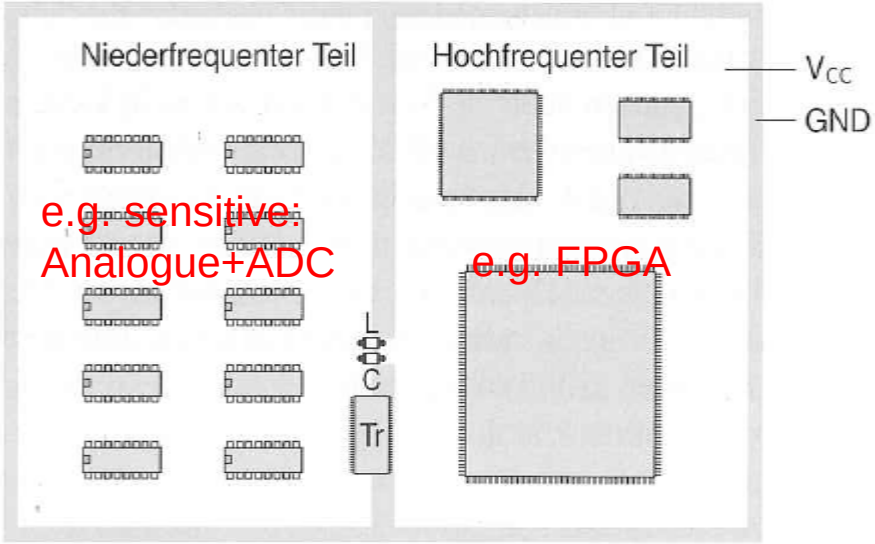


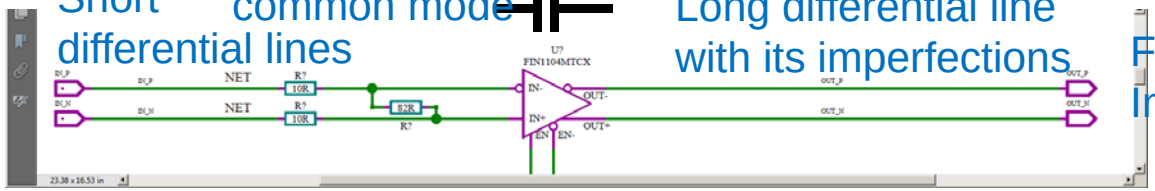
Signal and current transfer with high impedances.
Frequency range is: What the user limits it to

- Techniques to close currents

ADC

Short differential lines

Parasitic for common mode



Long differential line with its imperfections

FPGA, with its GND-bouncing,…
Imperfections of input loads

Methode: Current Loop analysis

Current loops cause disturbances by

- Common current on a line : One sees the current $I_{disturber}$ of the other as voltage U_{noise}
- Current loops generate B-Fields: Near fields “transformers” and far fields.

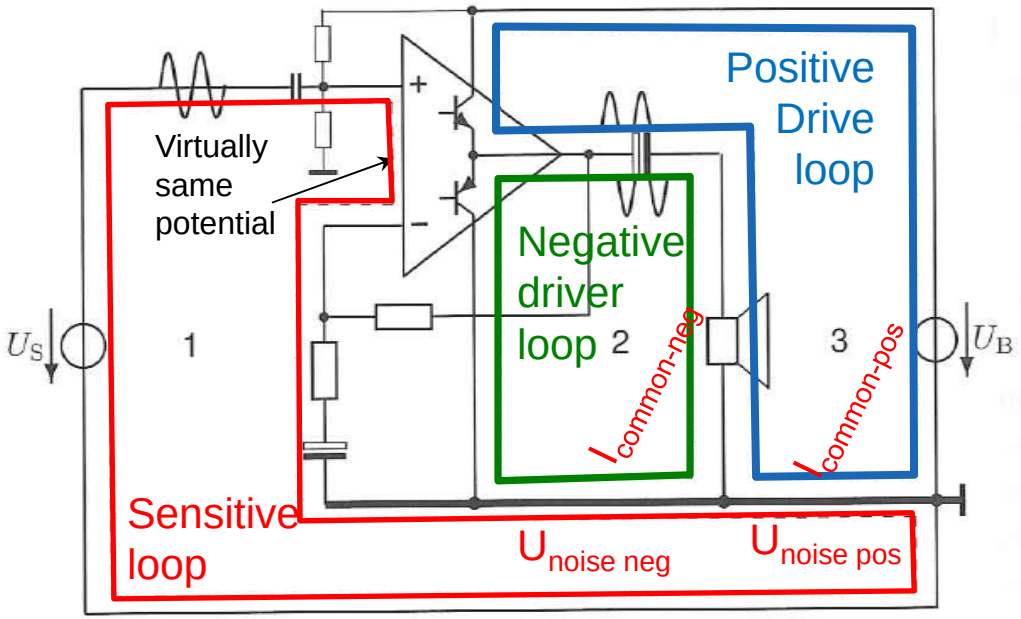


Bild 4.3: Stromanalyse an einer Verstärkerschaltung mit Differenzeingängen

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For MTCA the view

- DC paths
- Low frequency paths
- High frequency paths
- Field coupled paths

It includes always signal, power and GND.

Methode: Current Loop analysis, action

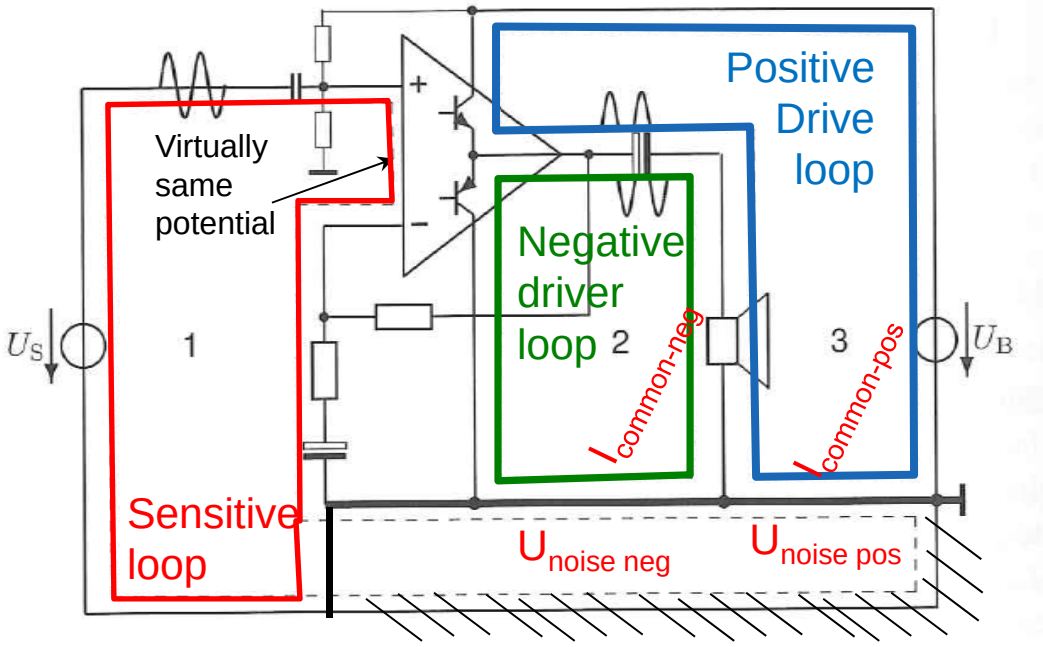

Bild 4.3: Stromanalyse an einer Verstärkerschaltung mit Differenzeingängen

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U_{noise} is no more in the sensitive loop

Methode: Current Loop analysis, action

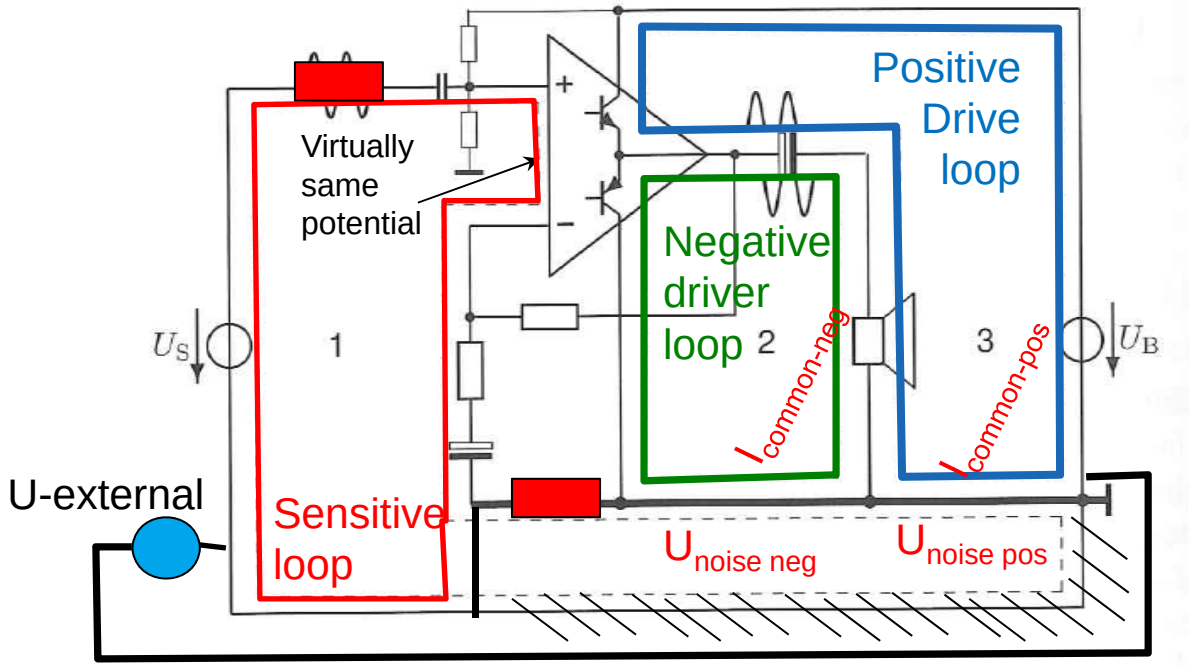

Bild 4.3: Stromanalyse an einer Verstärkerschaltung mit Differenzeingängen

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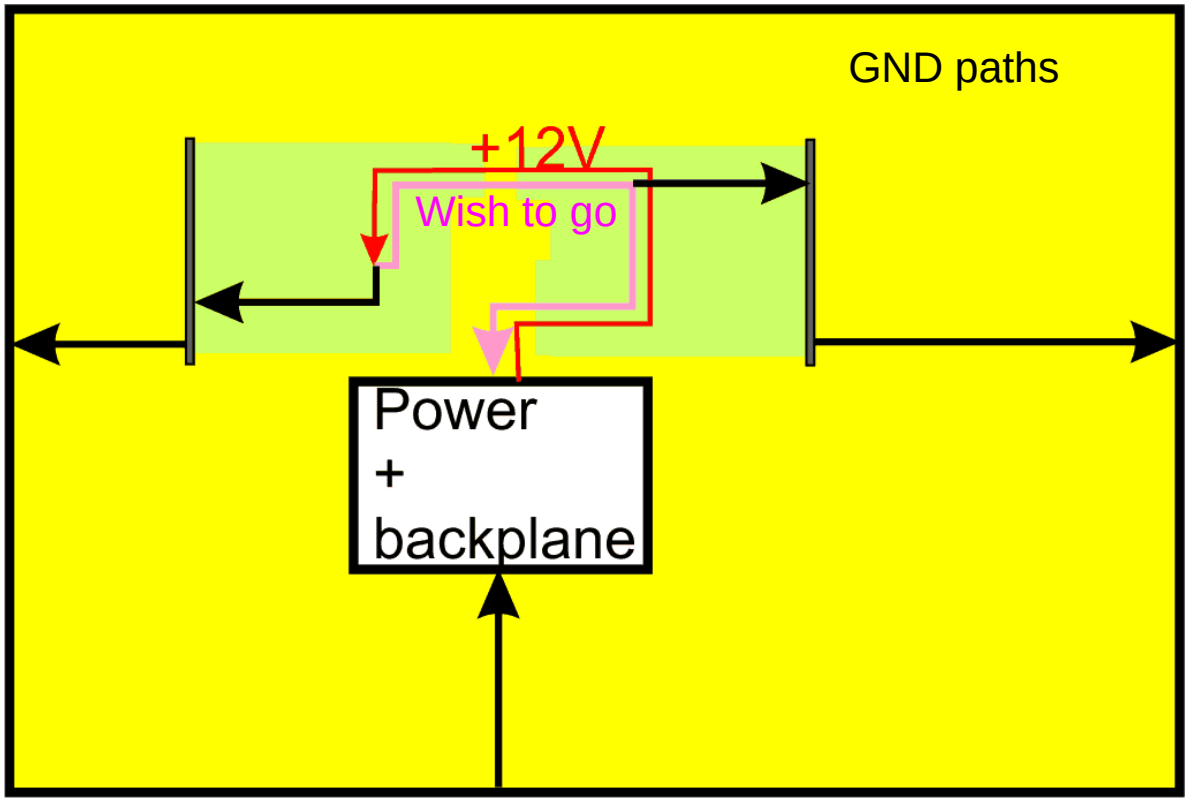
With more resistors
getting a differential
input stage
"cheap version of
instrumentation amplifier"

Less sensitive
to GND differences in larger
or high current systems

Current loops for sensitive parts has to be understood with planned currents and also the parasitic effects of components and field couplings.
None sensitives get into the game by common paths or fields.

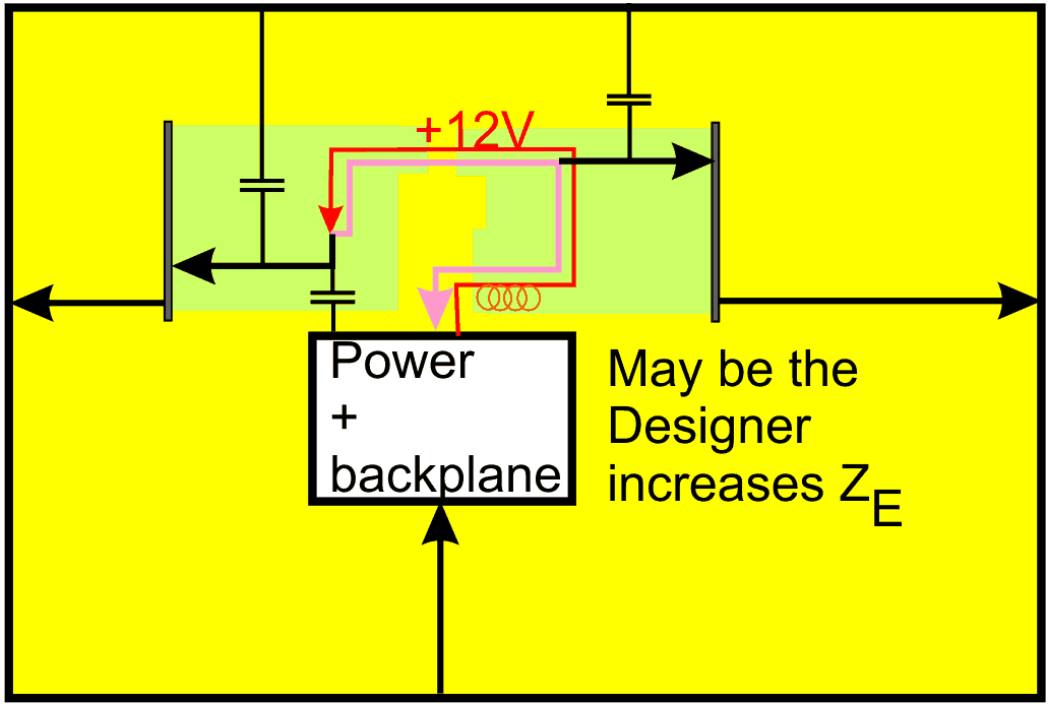
Current loop analysis in a simple crate: DC

GND system of two boads in a crate with metal chassis



DC currents will share by resistivity

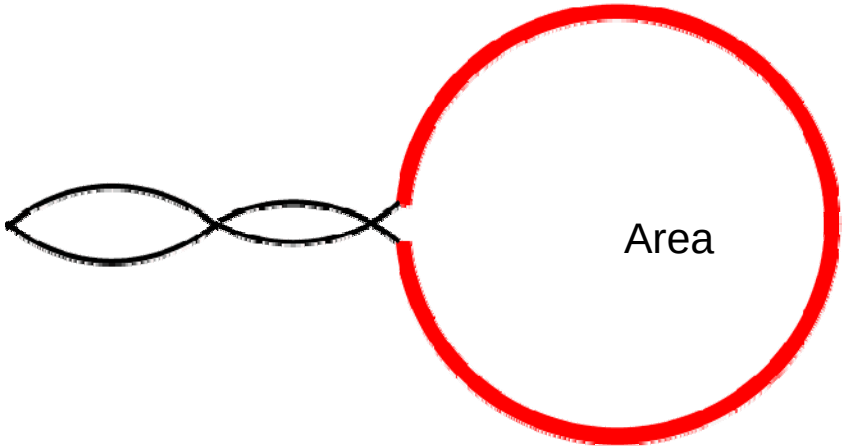
Current loop analysis in a simple crate: HF



Each loop gets an L_l
Each loop gets an impedance coupling
Capacitors between metal parts

Important by thinking: Identifying the important paths and loops
Simulations helps to prove and to quantify
CPU time : no simultaneous 3-dimensional and functional ;
guided simplification: What leaving away,
What simplified e.g. by R's, C's and L-matrix

What is DC , what is HF ?



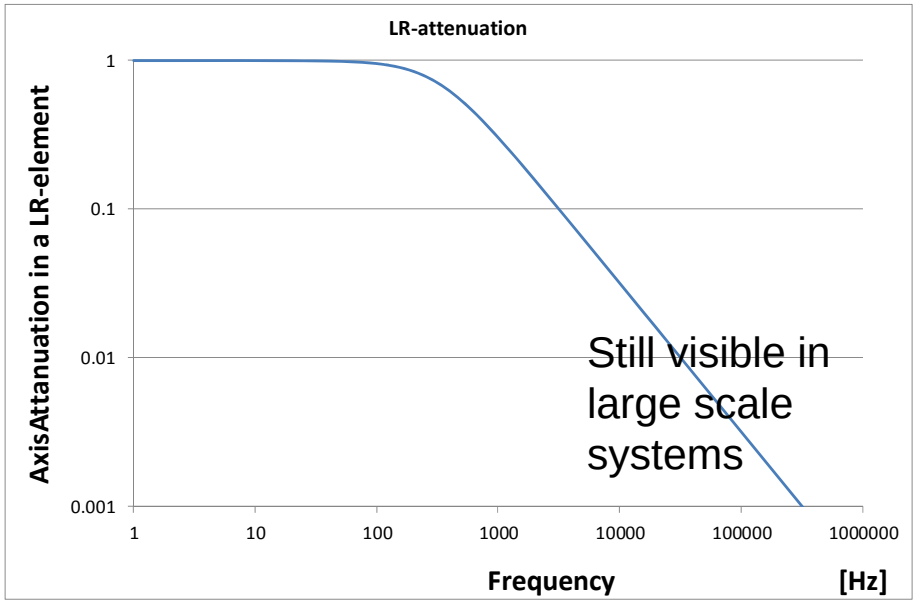
$$L = \frac{\mu_0}{2\sqrt{\pi}} \sqrt{Area} \ \ln \frac{Area}{\pi\,(wire\text{-}radius)^2}$$

60dB suppression at few 100kHz

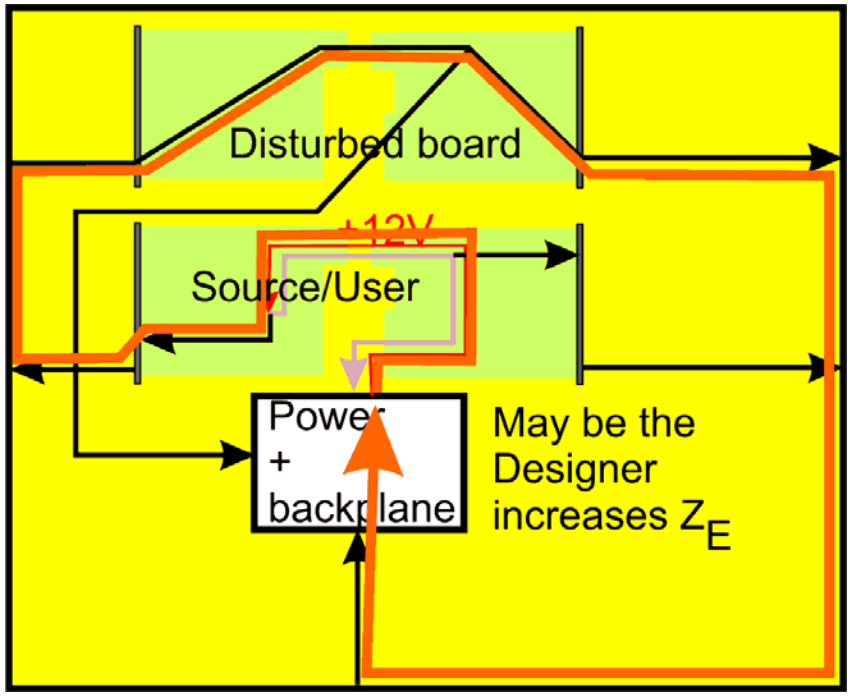
MTCA has ~50A at 12V
DC/DC 12V/~2.0V
factor 5 more within boards 250A
….. Blocking them by Z_K /Z_E?

EMI Planning: Approximations are sufficient
Guesses on area, small or large scale of rectangular
One of the time constant in the system is Inductance and Resistor : L/R

Typical scale for PCB is 200cm^2
and radii of the traces and wires <1mm:
L = 0.5µH
Typical resistors are 1mΩ
By that :
τ=0.5ms
Frequency: 1/(2πτ)=300Hz,
but: large attenuation is requested: L-R :



Dual user system



Far away from
"Every user is a zone"

Nice, if every user has a small Z_K

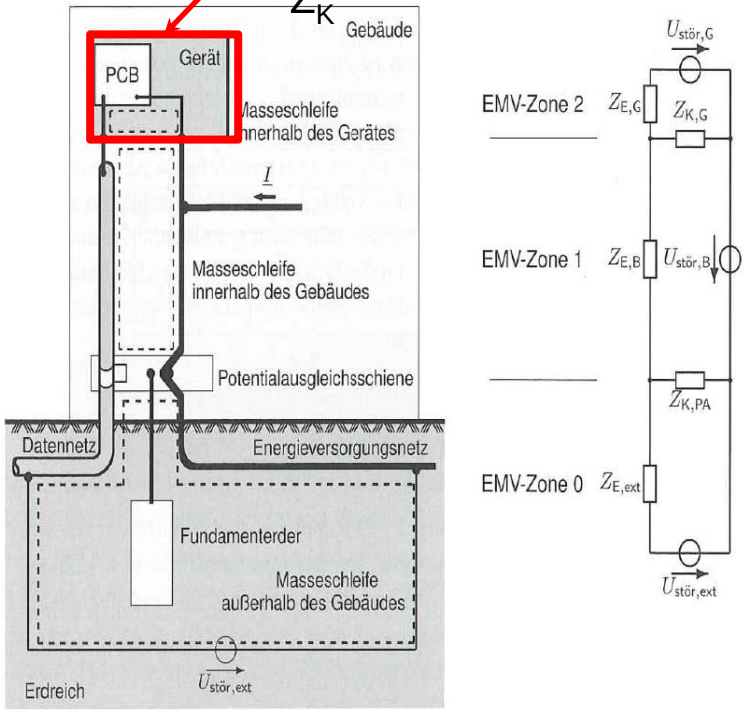


Bild 7.32: Masseschleifen in einer Anlage und ESB

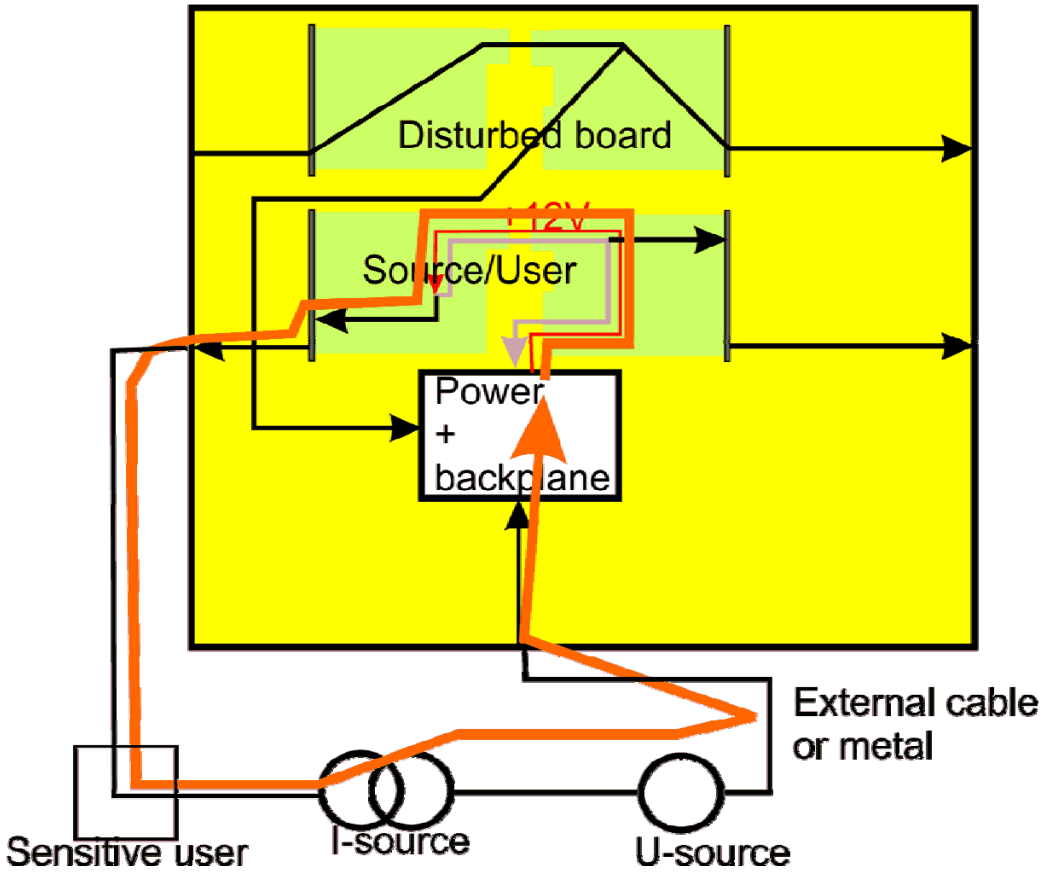
Current loop analysis with external User.

In the current loop analysis also the coupling to external is important, if not a small Z_K is foreseen.

Oneself can be the disturber and is sensitive to others.

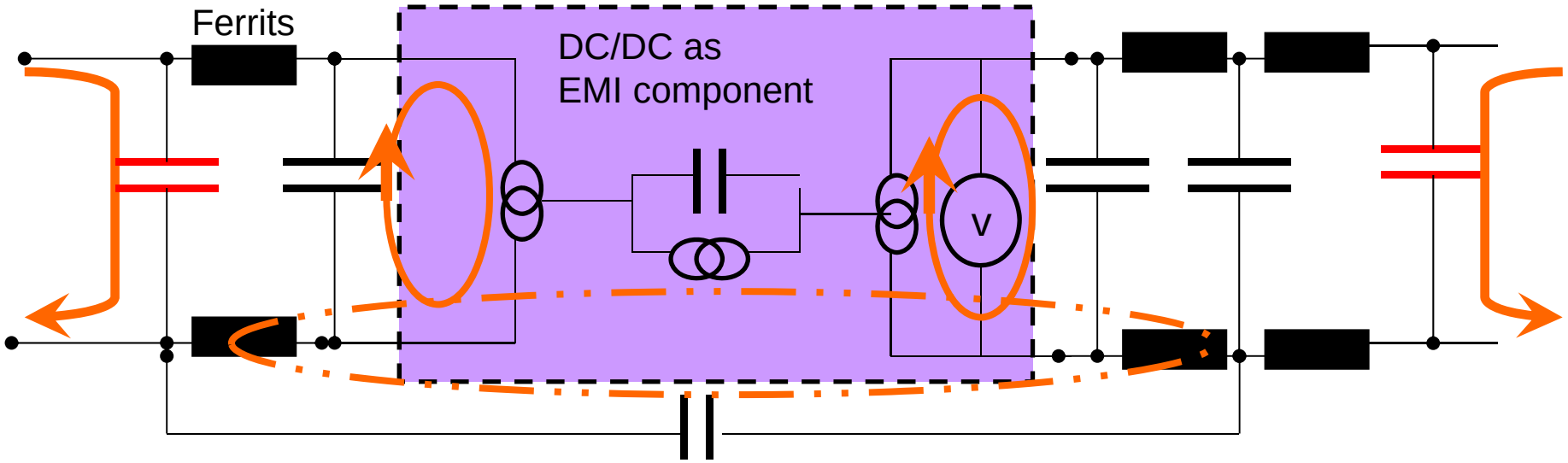
That correlation is not a “must” but likely.
If own performance is optimized by methods for individual effects, one might reach all stages:

- Good
- Disturber but not sensitive
- Sensitive but no disturber



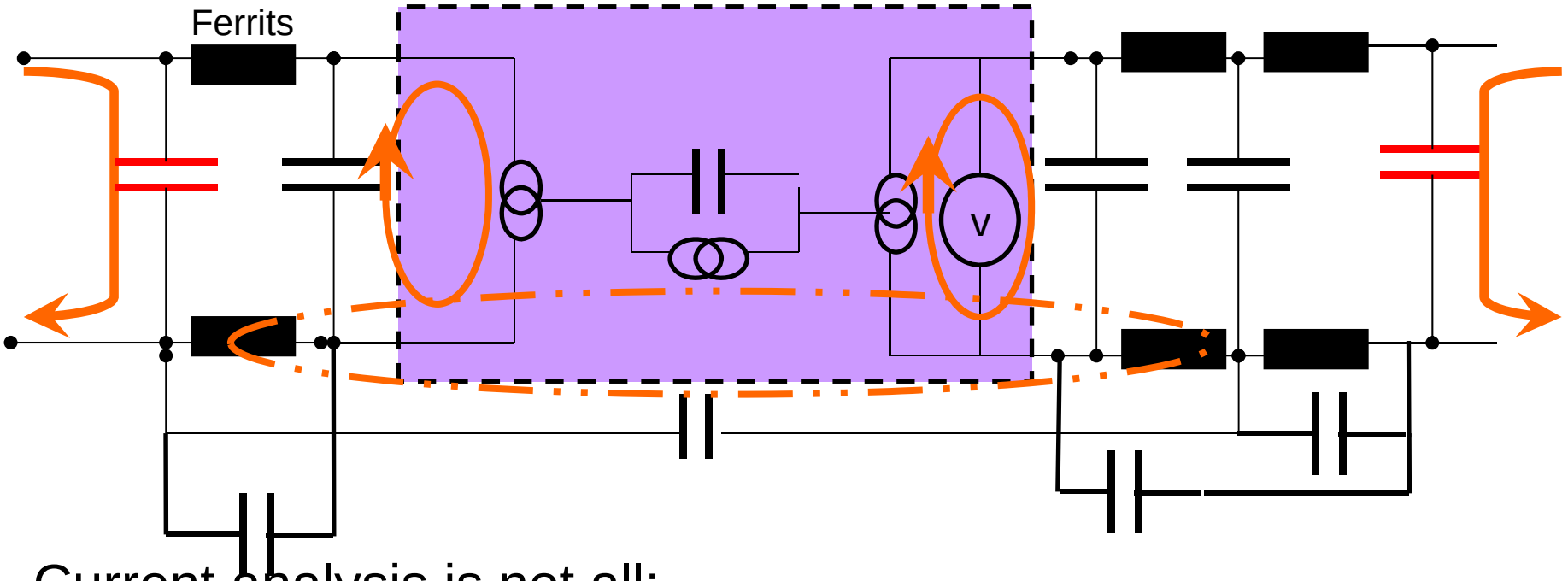
How to get a large Z_E and internal small Z_K

Example DC/DC converter: Disturber in the 10kHz to 1MHz and above to reach high efficiency by fast rise/fall-times



- Providing a short pass for each return current: Low L,R
- Designing the DC/DC+passives as zone,
  nearby leads for small Z_K or ferrites for a large Z_E

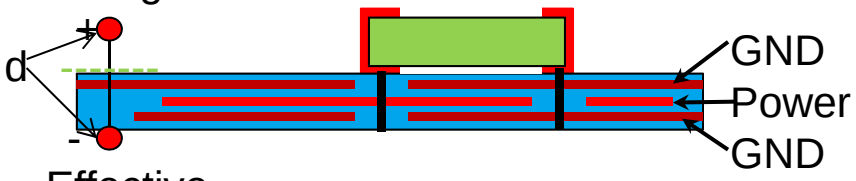
How to get a large Z_E and internal small Z_K: E-field?



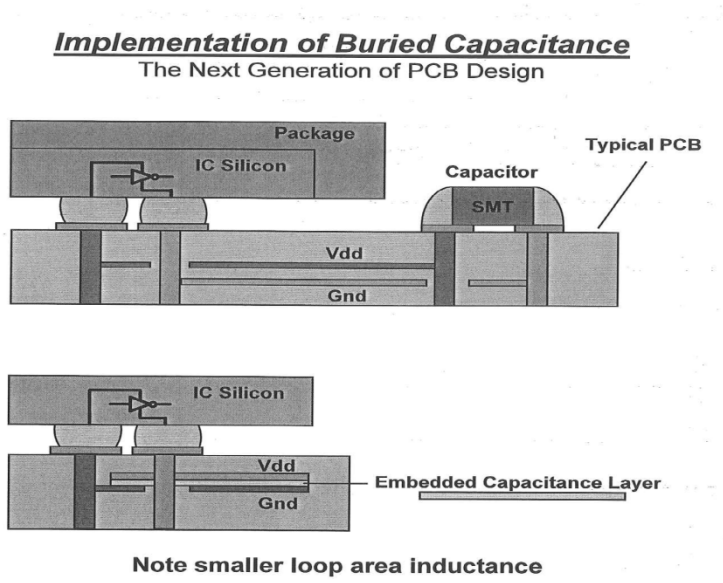
Current analysis is not all:
Making the DC/DC with large Decoupling, might convert currents into voltages and than E-fields.
Layout and usage dependent large islands might need a controlled E-field limitations for high frequencies.
Mostly better to shields or chassis than to electronic GND as Shown here.

E-field radiation

Field radiation by d/r^3, therefore mainly by high components or large floating areas



Effective mirror charge



E-field optimization, where needed:

- First inner layer as GND
  (Outer layer gains only 200µm, but most area is component.)
  If a lot of area on the outer layer is copper it radiates itself.
- Low height components, but not often allowed
- For components with its own switching currents, low impedance connections to GND needed
  Again “keeping the current loops small”

E-fields are able to be shielded by an external housing, additional effort

E-field radiation: Z_E, Z_K optimized system

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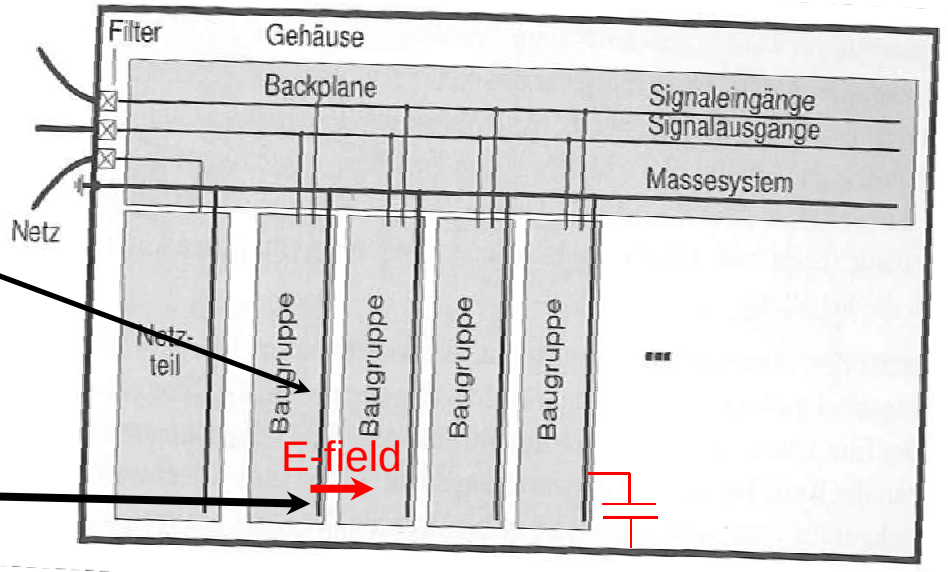
Current in that PCB generates Voltage drop

The part of the current, which is not locally under control will cause E-field radiation increasing to the end of the PCB



Effort needed? Design dependent

- Shields
- Planned grounding: Z(f)

- Zero coupling is never there, there is parasitic C's

- Agreements, what field at which geometrical position, returns to a "current planning"

B-field minimization

B-field is radiated by current loops and magnetic components

Component choice can minimize
Careful: E-Filed at top end is far away from GND-plane.

Similar differences for DC/DC ……..

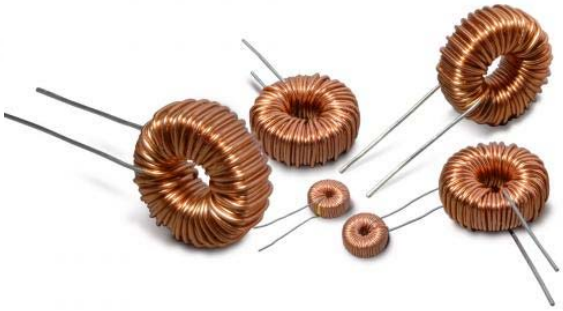
Near-field of B are very hard to shield:
Thickness of iron or ferrite needed
Its weight and its volumes growth with distance.

Mostly better

Solenoid
without return field
ferrite

Solenoid with
Return field ferrite

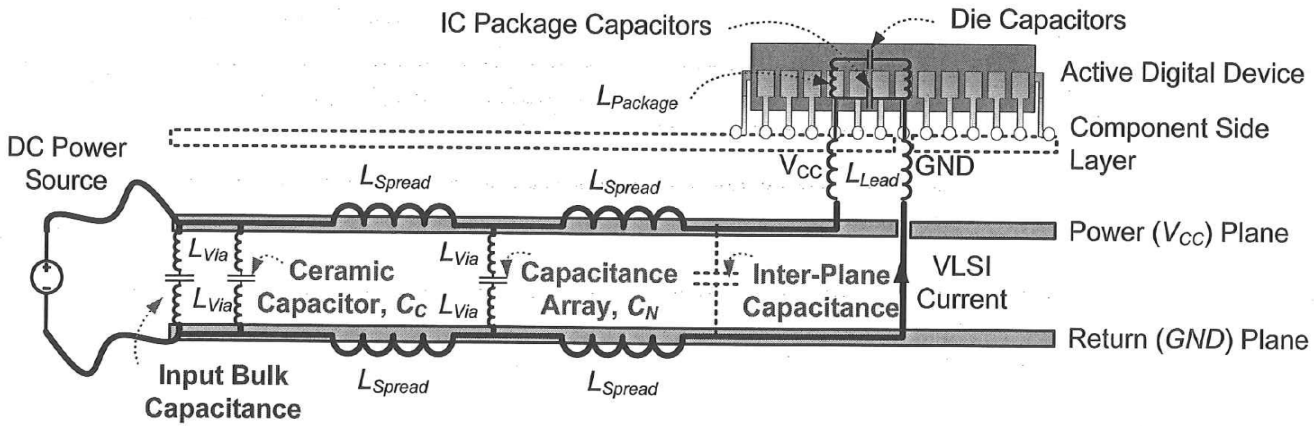
Toroid's behaves
like as one winding.



B-field and current loop avoidance in PCB design

B-field emmision and sensitivity depend beside components choice
- on a forced return path near supply path and
- on closing current loops locally

The Capacitor Brigade

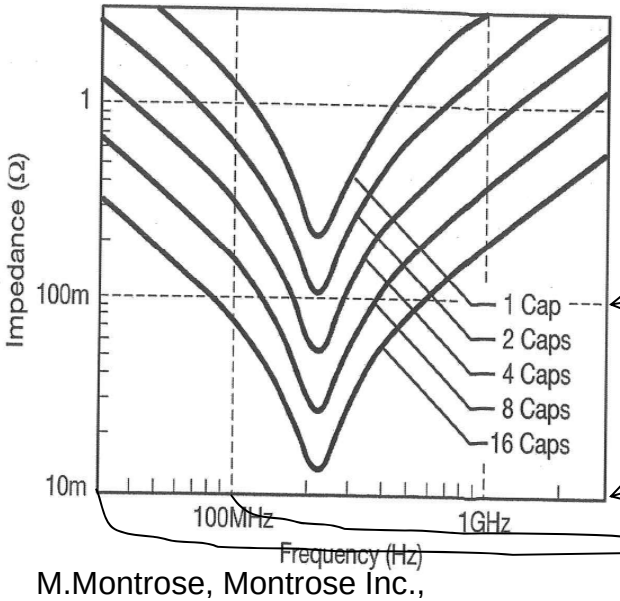


1. **The first surge of current come from the on-die capacitance.**
2. **The on-die capacitance is recharged from the package capacitance.**
3. **The package capacitance is recharged from the planes**
4. **The planes are recharged by the decoupling capacitor.**
5. **The decoupling capacitor is recharged by the planes.**
6. **The planes are then recharged by the bulk capacitor.**
7. **The bulk capacitor is recharged by the planes.**
8. **The planes are rechared by the power source.**

B-field and current loop avoidance in PCB design

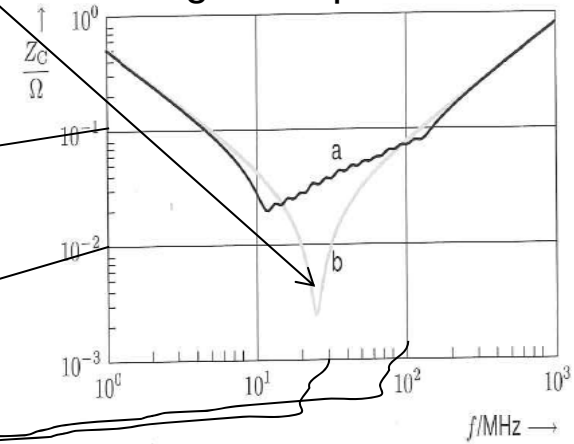
High frequency currents are only kept locally, by PCB
FR4: 50µm 60pF/cm^2 for power-GND-plane system

Blocking with parallel same type capacitors
+ only one type of capacitor
+ only risk of one serial resonance with layer capacitance
- Limited frequency band with lowest Z



M.Montrose, Montrose Inc., Santa Clara, USA

Blocking with different capacitors "broadband blocking"
- many different components while PCB population
- Higher risk of serial resonances between capacitors
+ Less risk of serial resonance with PCB
+ Wide range of low Z
+ Wider range with phase shift U_to_I≠90^0



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': Impedanz von 13 parallel geschalteten SMD-Kondensatoren, a: mit unterschiedlichen Kapazitätswerten nach der E6-Reihe, b: mit gleichen Kapazitätswerten

- I use normally the broadband blocking without bad experience
- Capacitors have no effect, if they are placed at the V-minimum of the PCB-resonances. Less minima at the circumference.

Field into receiving instrument?
Signal transfer differential or quasi differential

Industrial standards:

- LVDS … short distances 10-30m
- RS422/RS485: e.g. Ethernet in building
- Analog video signals , few 100MHz.
- 100-Ohm cables (4 pairs) ….

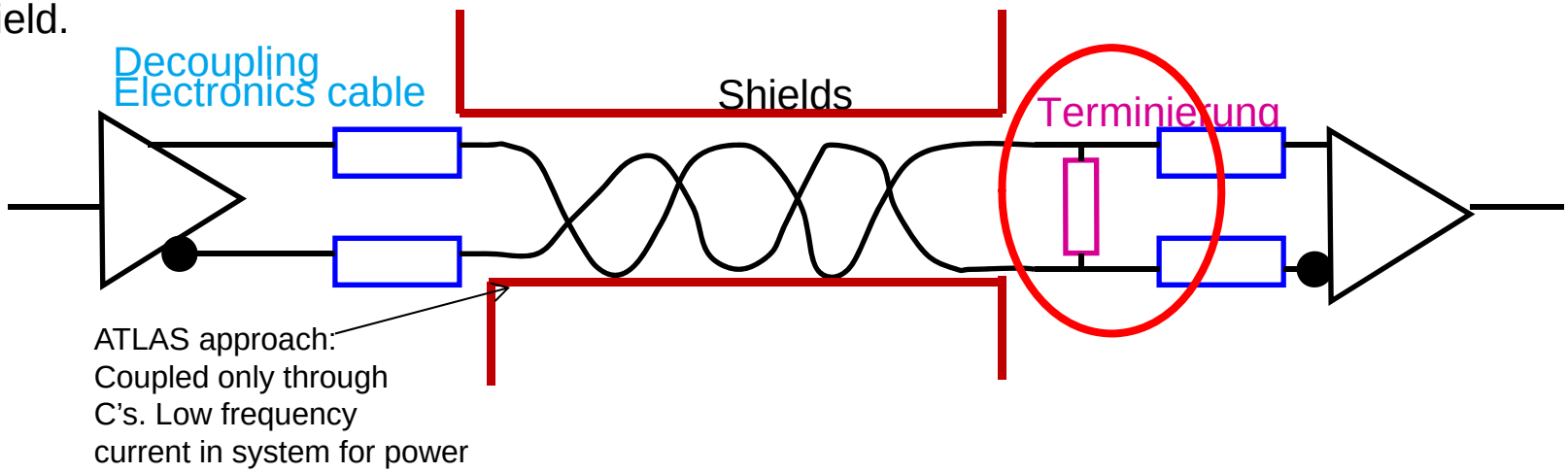
- No cheap single-pair, shielded, known, but 4pairs for LAN
- No standard connector for nuclear/X-ray research
- No Nuclear/X-ray specialized instruments.

That part radiates in the foreign EMI-zone:
To be kept small/shielded

- Limited disadvantage, because on the last meters of the cable the Common mode is dumped

Low frequency loop is broken high Z_E

Not available: Real RF, but RF likes to stay with the return current by itself in the nearby shield.



Also circuits for reasonable high output impedances are standardly used in analogue, IT

Providing a good current guide: Currents on cable shields

Cable shields should be connected at the entrance of the EMI zone.

Otherwise they are antennas inside
Alternative filter at that point

Low impedance connection, because AC/RF has build up on the cables.

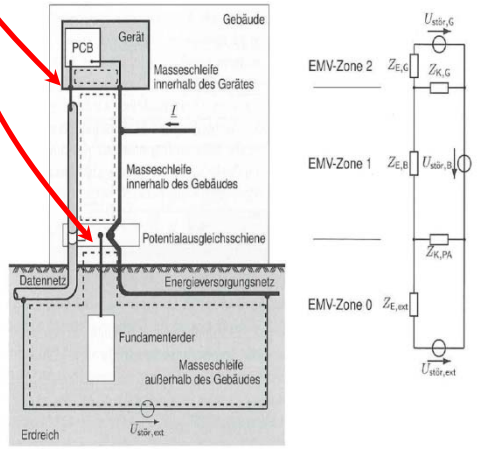
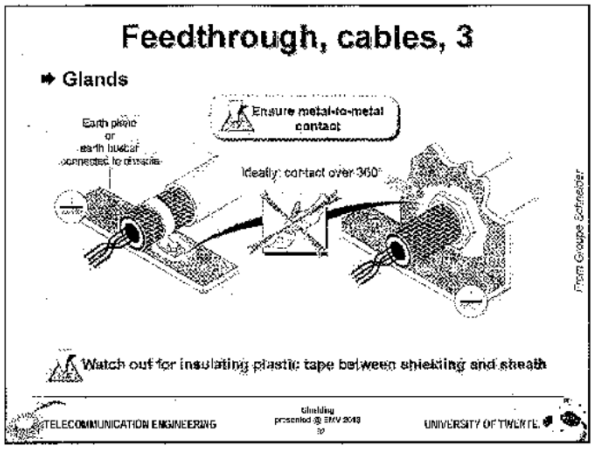
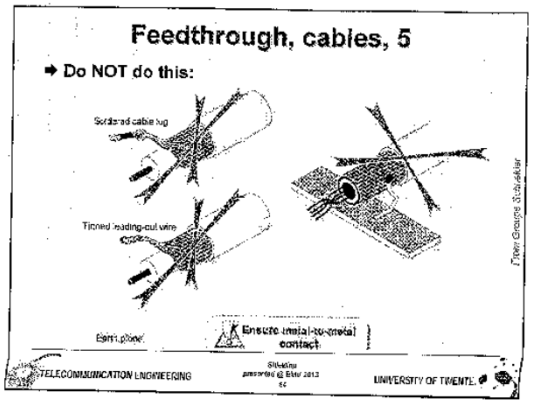


Bild 7.32: Masseschleifen in einer Anlage und ESB

Ideal



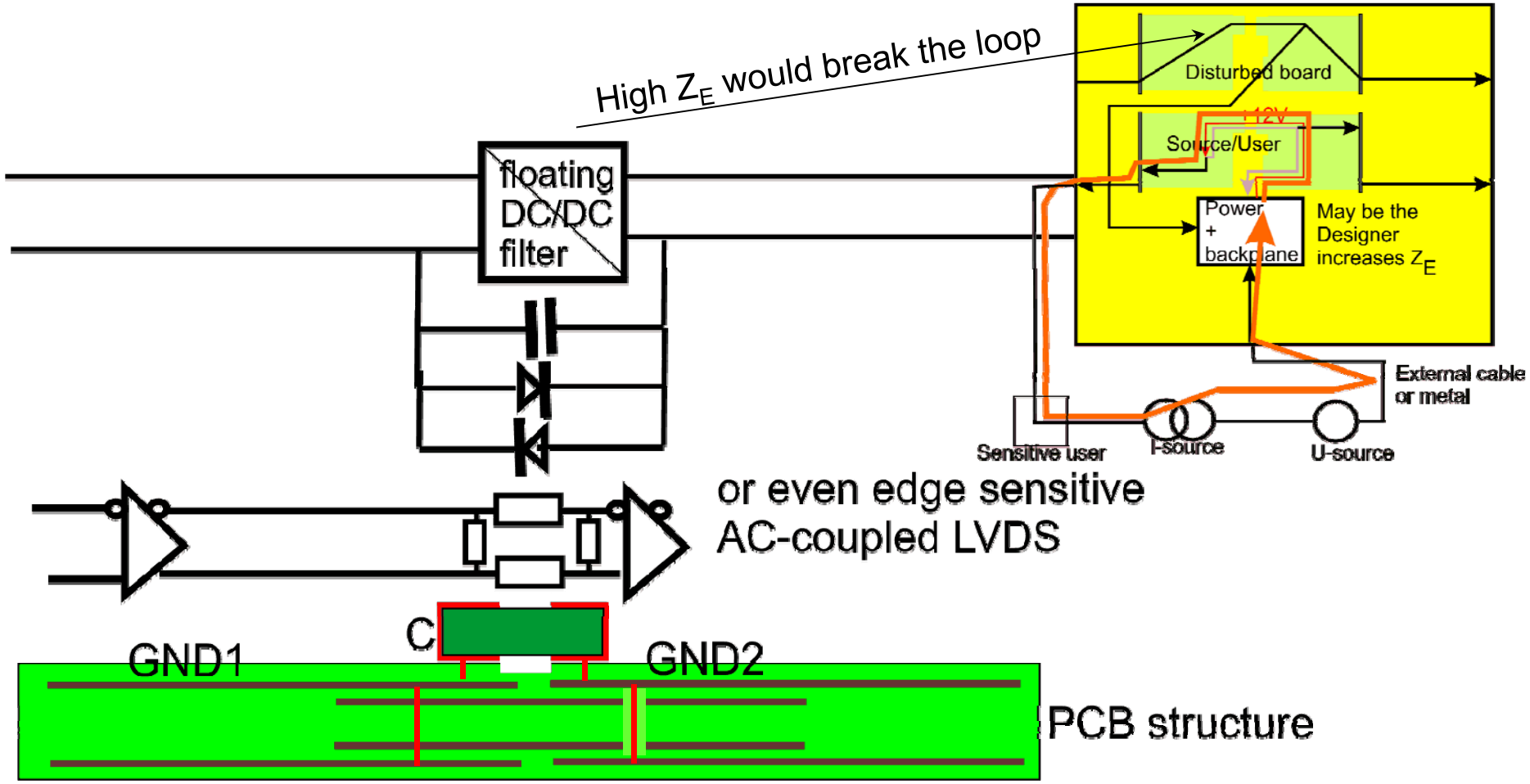
Bad, but not Useless



What is Practicable?
Try to minimize length.

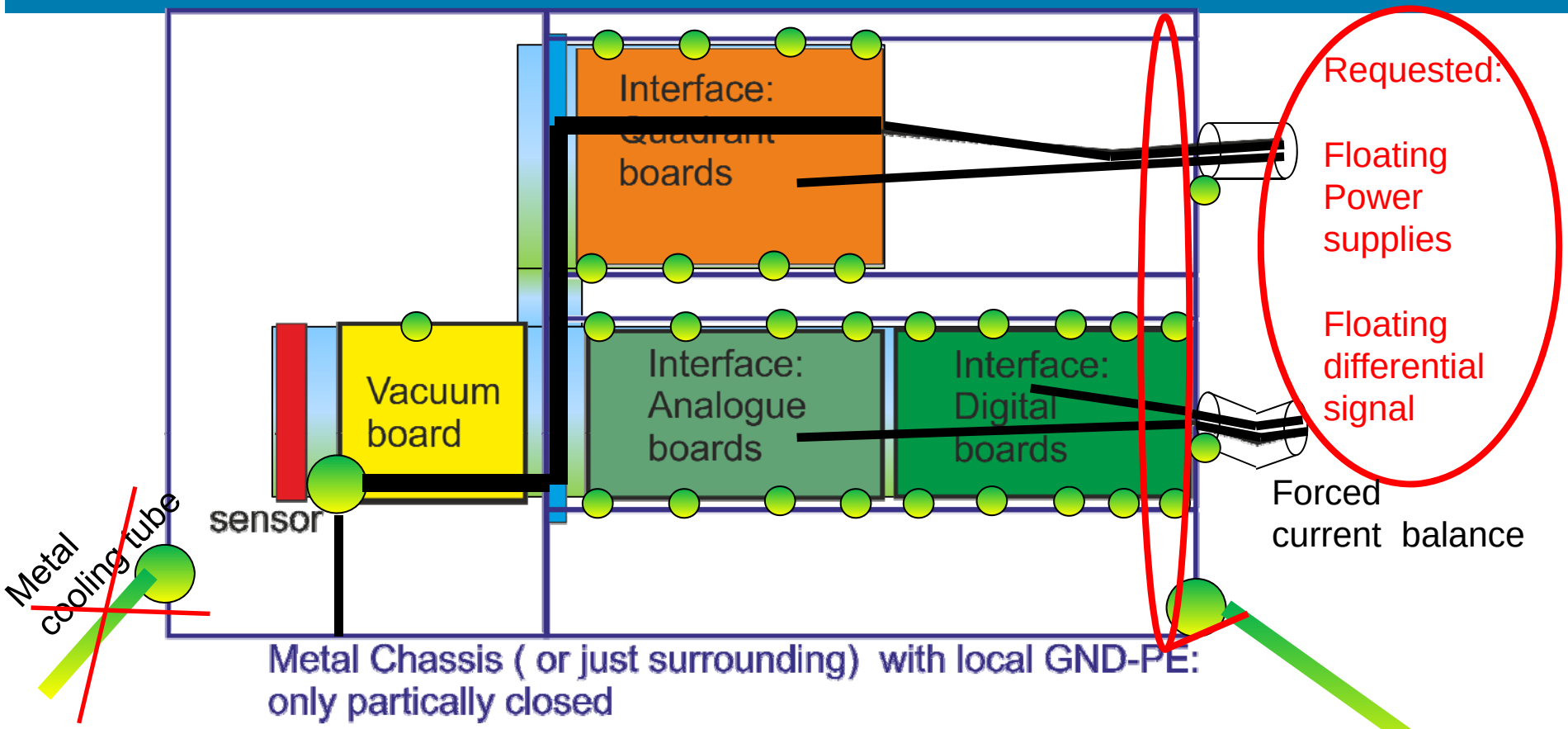
47

Example to get high Z_E in a Design/System



- Keep parasitic in mind
- Keep length of receiver short – imperfection just increase
- C's and diodes as the frequency coupling is wished for.

Keeping GND free of currents: AGIPD-plans



Using floating power supplies forces the currents to go to the power supply
Without using the general metal structures on PE.

Voltage drops on the metal of the detector are generated only by
the fraction of none controlled currents. They will be there!
⇒ They don't generate currents within the external metal PE system,
if only a small area provides the metal contacts to the outer world.

Summary

- EMI can be planned, not all problems will be identified
- Current loops need a well planning.
- (Hierarchical) EMI-zoning is advised
- Low coupling impedances Z_K have to be reached.

  Involved are all groups introducing designs with metal.
- Techniques for large decoupling impedances are available
  For RF?

- Signal standards helps to keep the noise low. RF