

SEDAC Video Switch

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1 General Remarks

- The module is a standard SEDAC Module
- Power consumption: ~ ? A @ 5 V.

The module is a video crossbar switch with 8 inputs and 4 outputs. Each of the 4 outputs can be connected to any of the 8 inputs (one at a time, no signal mixing) via SEDAC commands. Each output is capable of driving loads of 50 Ω , the bandwidth is 100 MHz (the switch used is the [MAXIM MAX458](#)).

1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

	Chip	Position
fpga logic	ACTEL 17E128	U4

2 SEDAC Connector (JSED)

The JIP is a standard 64 pin (2*32) connector (e.g. ERNI stv-b64-m-ab, DESY 29001). The signals written in *italic* are for reference only and will not be used on this module.

	a	b
1	<i>+24</i>	<i>+24</i>
2	<i>+24</i>	<i>+24</i>
3	GND	GND
4	GND	GND
5	<i>ANALOG</i>	<i>ANALOG</i>
6	PRD	GND
7	WT	GND
8	RDT*	RD
9	GND	WDT
10	GND	SDT
11	GND	XWT
12	GND	<i>XST*</i>
13	GND	SSA
14	<i>CP</i>	RSP*
15	-15	-15
16	-15	-15
17	<i>+15</i>	<i>+15</i>
18	<i>+15</i>	<i>+15</i>
19	<i>AC50Hz</i>	GND
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30	<i>RQ*</i>	<i>RQG</i>
31	VCC	VCC
32	VCC	VCC

3 SEDAC Subaddresses

SEDAC subaddress		+X'..'	READ	WRITE	BITS
7	6 5 4 3 2 1 0				
IOA	0 0	00	control output 0	control output 0	4
IOA	0 0	01	control output 1	control output 1	4
IOA	0 0	02	control output 2	control output 2	4
IOA	0 0	03	control output 3	control output 3	4

IOA: Module Base Address (bits 7...2)

3.1 Control Words

bits 15...4	bit 3	bits 2...0
0	Enable Output	Input Select

4 Revision History

- **10-Feb-99:** Revision 0