

# MPY Timing Module

Author: [Gerd Hochweller](#)

## 1 GENERAL REMARKS

### 1.1 DATA FILES FOR PROGRAMMABLE LOGIC

## 1 General Remarks

- The module is a eight slot wide VME format module (only the VCC and GROUND pins of the VME connectors are used).
- Power consumption: ~ ? A @ 5 V.

The module is basically a programmable crossbar switch with 8 clock inputs, 16 trigger inputs, 12 clock outputs and 12 trigger outputs. Each clock output may be delayed in 0.5 ns steps.

### 1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

	Chip	Position
<a href="#">fpga logic</a>	ACTEL 17E256	
<a href="#">clock switch</a>	MACH 220	
<a href="#">trigger switch</a>	MACH 220 (2*)	