Quad Multichannel Analyzer

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1 General Remarks

- The module is a one slot wide standard VME Module.
- The required VME address ranges are:
  16 bytes within the short address mode range **(A16, D16)**
  32 MB within the extended address mode range **(A32, D32)**.
- The VME base addresses are fixed within a PAL and therefore not switchable. If not specified otherwise the base addresses are:
  short acces mode: **0x1100**
  extended access mode: **0x08000000**.
- A standard 16 MB or 32 MB SIMM (60 ns)may be used.
- Power consumption: ~ ? A @ 5 V.

The module is used to readout and histogram the data from four completely independent datasources (like ADC's, TDC's, etc.). The data sources are connected to the front panel via standard 'Low Profile Header' connectors. Input J1 has 2*25 pins (e.g. 3M-3596-5002), the inputs J2, J3 and J4 have 2*13 pins (e.g. 3M-9593-5002). Each input can be configured for up to 256k channels (with 32 bits each). Double buffering may be used under program control, since two buffers are available for each device and VME access to the memory is possible during data taking.
In the current version the four inputs are configured for

- J1: LeCroy TDC4208 (modified, 256k channels)
- J2, J3, J4: LeCroy TDC4201 (modified, 64k channels)

Since the configuration is daone in a XILINX chip it may be changed (as long as certain limitations are fulfilled).

1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

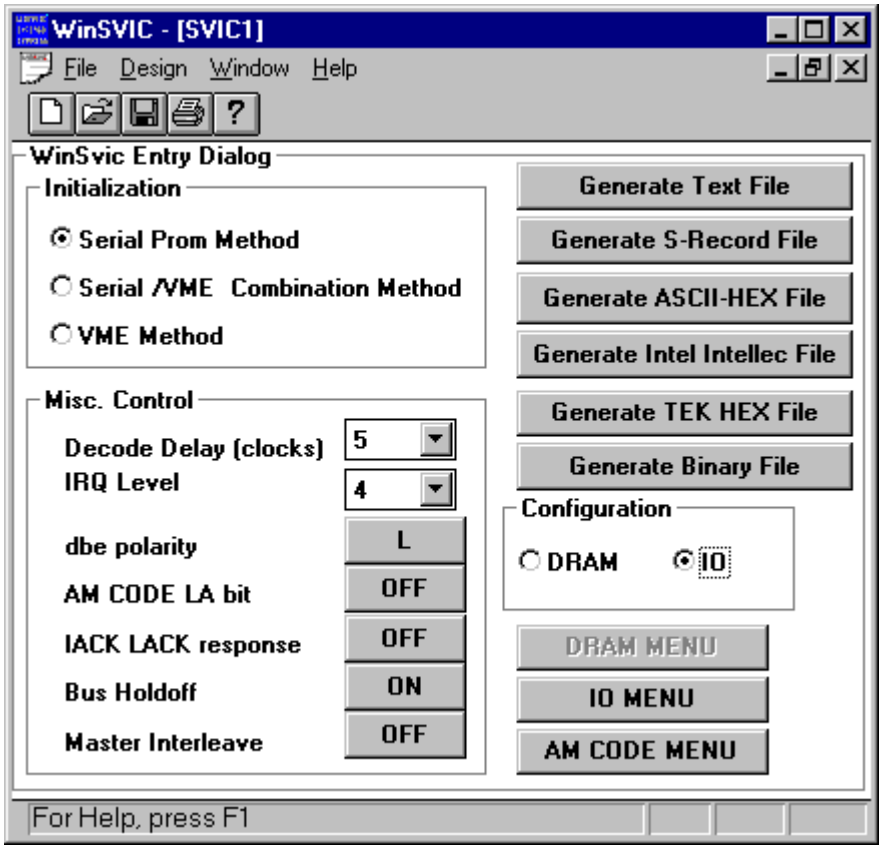
	Chip	Position
VME configuration	ACTEL AT17E65	FEA_VME_P1
VME baseaddr	AMD PALCE22V10	U11
fpga logic	ACTEL 17E256	U12

2 VME Interface

2.1 Configuration

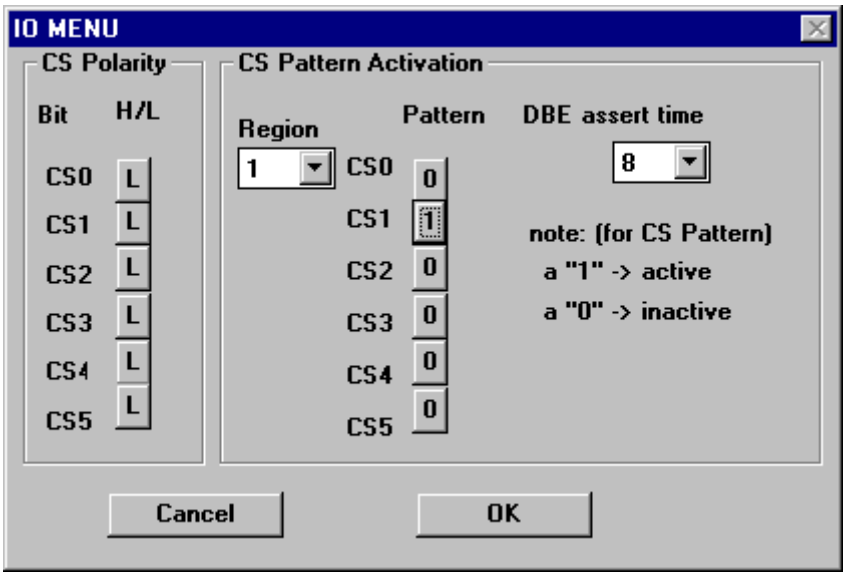
To access the VME bus the standard FEA mezzanine boards 'FEA-VME-P1' and 'FEA-VME-P2' are used. The modules have to be configured via a serial EEPROM ACTEL 'AT17E65' The configuration data are generated with the the program 'WinSVIC' (Cypress).

2.1.1 Common Part

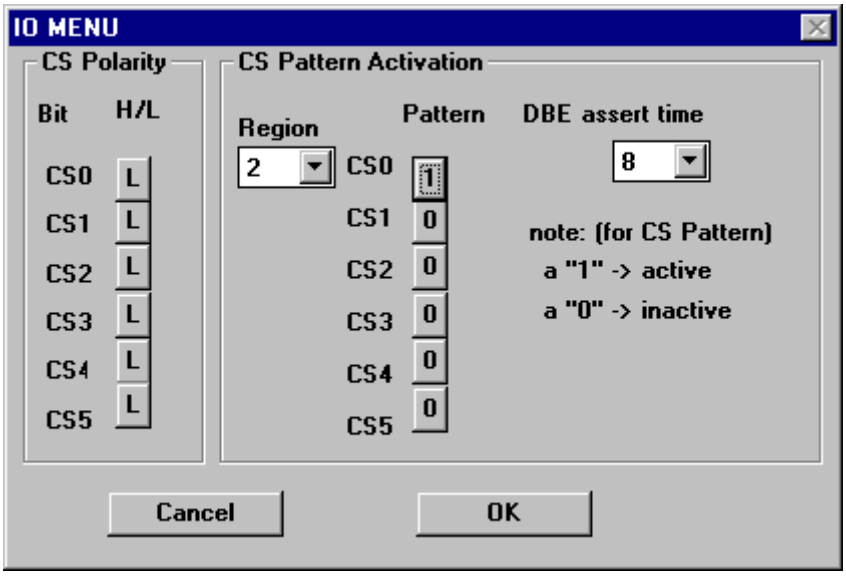


2.1.2 IO MENU Specifications

The interface supports two different regions.
The Region 1 (input signal REG0_) is used for the control commands:

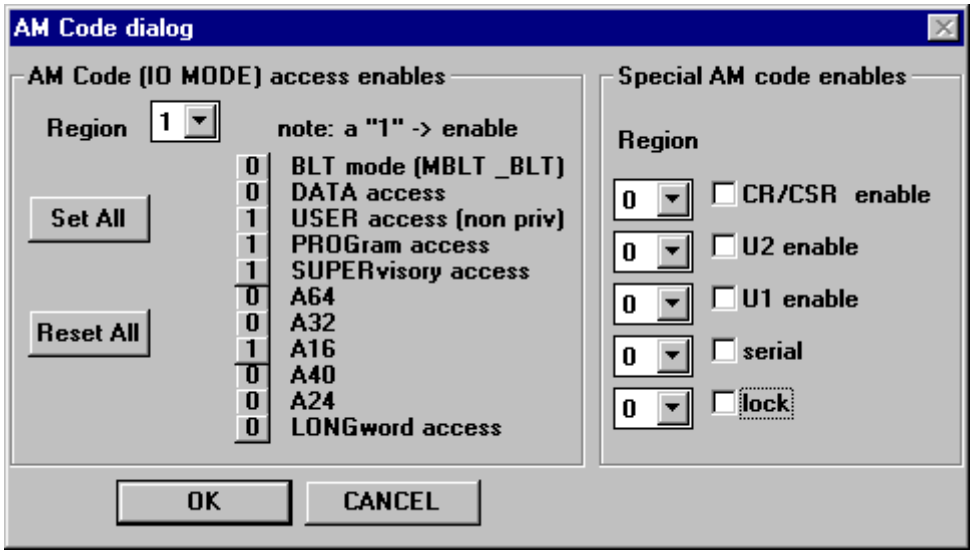


The Region 2 (input signal REG1_) is used for the memory access:

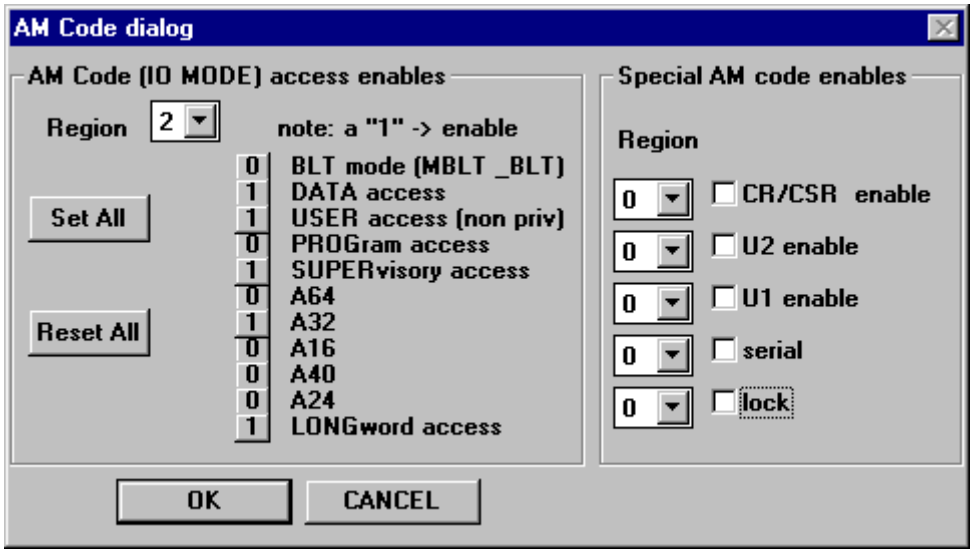


2.1.3 AM CODE MENU Specifications

The control command (Region 1) use the A16 / D16 mode (AM codes '29' and '2D'):



The memory access command (Region 2) use the A32 / D32 mode (AM codes '09' and '0D')



2.2 Control Commands

The control commands use the VME short access mode and 16 bit data words (**A16, D16**).

VME address 15-4 3 2 1 0	+X'..'	READ	WRITE	BITS
IOA 0 0 . 0	00	Mode dev 1	mode dev 1	2
IOA 0 1 . 0	04	Mode dev 2	mode dev 2	2
IOA 1 0 . 0	08	Mode dev 3	mode dev 3	2
IOA 1 1 . 0	0C	Mode dev 4	mode dev 4	2

IOA: VME base address IO access (bits 15...4)
'.': don't care (not decoded)

mode bits 15-2: not used
1: 0 = input to buffer 0
1 = input to buffer 1
0: 0 = run stopped
1 = run started

2.3 Memory Access

The memory access commands use the VME extended access mode and 32 bit data words (**A32, D32**). A standard 72 pin SIMM (16 MB or 32 MB, 60 ns) can be used. The memory can be written (for reset and test purposes) and may be read out at any time (even during data input). In the current version the memory contains 8 buffers at the following addresses:

VME address range MEA + X'..'		buffer size (32 bit words)
000000 .. 0FFFFC	device 1, buffer 0	256 k
100000 .. 1FFFFC	device 1, buffer 1	256 k
200000 .. 23FFFC	device 2, buffer 0	64 k
300000 .. 33FFFC	device 2, buffer 1	64 k
400000 .. 43FFFC	device 3, buffer 0	64 k
500000 .. 53FFFC	device 3, buffer 1	64 k
600000 .. 63FFFC	device 4, buffer 0	64 k
700000 .. 73FFFC	device 4, buffer 1	64 k

MEA: VME base address memory access (bits 31...25)

3 Data Source Connectors

3.1 Device 1 (J1)

The J1 connector is a standard 50 pin (2*25) 'Low Profile Header' (e.g. 3M-N-2550-5002).

Pin	Signal		Pin	Signal
1	DATA RDY*		2	
3	DATA ACK*		4	
5			6	
7			8	
9			10	
11			12	
13			14	
15			16	DATA BIT 17
17			18	DATA BIT 16
19			20	DATA BIT 15
21			22	DATA BIT 14
23			24	DATA BIT 13
25			26	DATA BIT 12
27			28	DATA BIT 11
29			30	DATA BIT 10
31			32	DATA BIT 9
33			34	DATA BIT 8
35			36	DATA BIT 7
37			38	DATA BIT 6
39			40	DATA BIT 5
41			42	DATA BIT 4
43			44	DATA BIT 3
45			46	DATA BIT 2
47			48	DATA BIT 1
49			50	DATA BIT 0

The following diagram shows the data transfer handshake timing for device 1. Data will be strobed into the latches by the trailing edge of 'DATA RDY*'.

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3.2 Devices 2, 3, 4 (J2, J3, J4)

The J2, J3, J4 connectors are standard 26 pin (2*13) 'Low Profile Headers' (e.g. 3M-N-2526-5002).

Pin	Signal		Pin	Signal
1	DATA ACK		**2**	DATA RDY*
3	DATA BIT 0		**4**	DATA BIT 1
5	DATA BIT 2		**6**	DATA BIT 3
7	DATA BIT 4		**8**	DATA BIT 5
9	DATA BIT 6		**10**	DATA BIT 7
11	DATA BIT 8		**12**	DATA BIT 9
13	DATA BIT 10		**14**	DATA BIT 11
15	DATA BIT 12		**16**	DATA BIT 13
17	DATA BIT 14		**18**	DATA BIT 15
19	*(DATA BIT 16)*		**20**	*(DATA BIT 17)*
21			**22**	
23			**24**	
25			**26**	

The following diagram shows the data transfer handshake timing for devices 2, 3, 4. Data will be strobed into the latches by the leading edge of 'DATA ACK'.

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4 Revision History

- **23-Jun-99:** version 1