ADC Canberra-8701 Multichannel Analyzer

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1 General Remarks

- The module is a single-size IP Module (8 MHz)
- Power consumption: ~ ? A @ 5 V.

The module is used to control and readout a Model 8701 ADC (Canberra Industries) via an IP-Bus Carrier Board.
The Model 8701 is a 100 MHz Wilkinson ADC with 8192 channels of resolution. The IP Module provides the logic and the memory to establish a multichannel analyzer with 8192 channels and 32 bits for each channel.
The memory is divided into two parts (MEMA and MEMB), each of those can hold 8192 channels (32 bits each). While the ADC fills one memory part the other one may be accessed via the IP bus. If the same memory part which is used by the ADC is accessed via the IP bus at the same time there is a very small chance that an error occurs (the dual port memory does not allow to access the same memory location from both ports at the same time).
In test mode the three ADC control signals (READY*, INB*, ACEPT*) are under software control and are not handled by the hardware.
The actual revision of the board can be found in word 6 of the ID PROM. The latest revision is **1.**

1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

	Chip	Position
fpga logic	ACTEL 17E256	U1

2 IP Connector (JIP)

The JIP is a standard 50 pin (2*25) connector (e.g. AMP 173279-3). The signals written in *italic* are for reference only and will not be used on this module.

Pin	Signal		Pin	Signal
1	GND		**2**	CLK
3	RESET*		**4**	D0
5	D1		**6**	D2
7	D3		**8**	D4
9	D5		**10**	D6
11	D7		**12**	D8
13	D9		**14**	D10
15	D11		**16**	D12
17	D13		**18**	D14
19	D15		**20**	*BS0**
21	*BS1**		**22**	*-12V*
23	*+12V*		**24**	+5V
25	GND		**26**	GND
27	+5V		**28**	R/W*
29	IDSel*		**30**	*DMAReq0**
31	MemSel*		**32**	*DMAReq1**
33	*IntSel**		**34**	*DMAAck**
35	IOSel*		**36**	*reserved*
37	A1		**38**	*DMAEnd**
39	A2		**40**	*Error**
41	A3		**42**	*IntReq0**
43	A4		**44**	*IntReq1**
45	A5		**46**	*Strobe**
47	A6		**48**	Ack*
49	*reserved*		**50**	GND

3 ADC Connector (JADC)

The JADC is a standard 50 pin (2*25) connector (e.g. AMP 173279-3). The signals written in *italic* are for reference only and will not be used on this module.

Pin	Signal		Pin	Signal
1	GND		**2**	ACEPT*
3	GND		**4**	ENDATA*
5	GND		**6**	*CDT**
7	GND		**8**	ENC*
9	GND		**10**	READY*
11	GND		**12**	INB*
13	*reserved*		**14**	ADC00*
15	ADC07*		**16**	ADC01*
17	ADC08*		**18**	ADC02*
19	ADC09*		**20**	ADC03*
21	ADC10*		**22**	ADC04*
23	ADC11*		**24**	ADC05*
25	ADC12*		**26**	ADC06*
27	*reserved*		**28**	*reserved*
29	*BF**		**30**	VGAIN
31	*BLLD*		**32**	VZERO
33	*BCB**		**34**	*reserved*
35			**36**	
37			**38**	
39			**40**	
41			**42**	
43			**44**	
45			**46**	
47			**48**	
49			**50**	

4 IP Addresses

VME address 15 14-7 6 5 4 3 2 1 0	+X'..'	READ	WRITE	BITS
IOA 0 0 0	00	control bits	control bits	3
IOA 0 1 0	02	MEMA status	reset MEMA status	4/0
IOA 1 0 0	04	MEMB status	reset MEMB status	4/0
IOA 1 1 0	06	ADC register	ADC register	15
MEA 0 x x x x x x 0 0		MEMA low order	MEMA low order	16
MEA 0 x x x x x x 1 0		MEMA high order	MEMA high order	16
MEA 1 x x x x x x 0 0		MEMB low order	MEMB low order	16
MEA 1 x x x x x x 1 0		MEMB high order	MEMB high order	16

IOA: VME base address IP IO access (bits > 6)
MEA: VME base address IP memory access (bits > 15)
'x': used bits
'.': don't care (not decoded)

4.1 Control Bits

BIT	READ	WRITE
X'0001'	Memory Select	Memory Select
X'0002'	RUN	RUN
X'0004'	Test Mode	Test Mode

Memory Select: **0:** use MEMA
1: use MEMB
RUN: **0:** disable ADC
1: enable ADC
Test Mode: **0:** normal mode
1: test mode

The 'Memory Select' and 'Test Mode' bits are valid only if the 'RUN' bit is switched on.

4.2 Status Bits (MEMA or MEMB)

BIT	READ	WRITE
X'0001'	memory in use by ADC	---
X'0002'	memory in use by ADC (test mode)	---
X'0004'	memory contains data	---
X'0008'	invalid data detected	---

The 'memory contains data' and 'invalid data detected' bits are latches. They are cleared if the 'RUN' bit is switched on, i.e. 'invalid data detected' means that at least one invalid data value has been detected during the run.

4.3 ADC register

BIT	READ	WRITE
X'1FFF'...X'0000'	ADC data	---
X'2000'	data invalid (INB*)	---
X'4000'	data available (READY*)	---
X'8000'	0	data accepted (ACEPT*)

5 IP Module ID Prom

The ID prom supports the first 16 words of the standard data format I.

WORD	
0	"I"
1	"P"
2	"A"
3	"C"
4	1
5	2
6	Revision
7	0
8	0
9	0
10	16
11	0
12	"F"
13	"E"
14	"A"
15	" "

6 Revision History

- **15-Oct-98:** minor changes (manual only)
- **10-Nov-98:** high and low order data address corrected (revision: **1**)