ANGIO Receiver Test Module

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1 General Remarks

- The module standard VME Module (no bus connection, power only).
- Power consumption: ~ ? A @ 5 V.

The module is used for testing of the ANGIO Receiver module. It contains a memory which can hold one double line of ANGIO pixel data. This memory can be written from the ANGIO receiver module via the fiber link under program control. Once the line memory has been filled this information can be transferred (n-times) using the same timing as the actual ANGIO detector readout.

1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

	Chip	Position
fpga logic	ACTEL 17E128	U6

2 Write Fiber Link Data Format

The data must be sent to the test module in the same order they are to be received later by the receiver module (i.e. normally the pixel line format of the ANGIO detector, see ANGIO Detector Module).
The format of the fiber link data word transferred to the test module is the following (the bit 15 ist the 'data valid bit' and will be inserted by hardware):

bit 14	bit 13	bit 12	bits 11...0	action
overflow	0	'SYNC' and 'DEAD'	pixel data	write data into next memory address
---	1	0	---	reset memory address
---	1	1	line count	transfer line 'line count' times