ZEUS Luminosity Monitor

Backplane

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1 General Remarks

- The backplane (board number DESY-FEA 7254) has been especially designed for the ZEUS Luminosity Monitor Crate.
- It is used as an additional backplane on top of the standard VME64 P2 backplane (HARTING connectors).
- The backplane is connected to the VME slots 6 ... 21.

2 Backplane Pin Assignments

Of the connector row 'b' only the standard 'VCC' and 'GND' pins are connected to the backplane.

The clock signal '**HC1/HC1***' is connected to slots 8...11 (terminated with 100 Ω at slot 11).
The clock signal '**HC2/HC2***' is connected to slots 12...15 (terminated with 100 Ω at slot 15).
The clock signal '**HC3/HC3***' is connected to slots 16...18 (terminated with 100 Ω at slot 18).
The clock signal '**HC4/HC4***' is connected to slots 19...21 (terminated with 100 Ω at slot 21).

'**T**' is a standard termination (330 Ω against VCC and 470 Ω against GND) and used for the signals
'**TRG00**' **...** '**TRG15**', '**RSV0**', '**RSV1**' at both ends (slots 6 and 21)
'**BCN0**', '**ACCEPT**', '**BANK**' at one end only (slot 21).
All other lines are not terminated on the backplane.

The signals '**SUM8/SUM8***' **...** '**SUM21/SUM21***' must be terminatd (27 Ω) on the trigger board.
The signal '**NOBUF***' is an open collector TTL signal and must have a pullup on the trigger board.

The current usage of the signals 'TRG00' ... 'TRG15' is the following:

TRG00: GFLT (First Level Trigger Event Flag)
TRG01: INCA (increment Ram Address)
TRG02: MRES (Module Reset)
TRG03: n.u
..
TRG15: n.u.

	slots 6 + 7						slot 8				...	slot 21					
	z		a		c	d	z	a	c	d		z		a		c	c
1	T	TRG00		HC1			TRG00	HC1				TRG00	T	HC4			
2		GND		HC1*			GND	HC1*				GND		HC4*			
3	T	TRG01		HC2	SUM21	VLD21*	TRG01					TRG01	T				
4		GND		HC2*	SUM21*		GND					GND					
5	T	TRG02		HC3	SUM20	VLD20*	TRG02					TRG02	T				
6		GND		HC3*	SUM20*		GND					GND					
7	T	TRG03		HC4	SUM19	VLD19*	TRG03					TRG03	T				
8		GND		HC4*	SUM19*		GND					GND					
9	T	TRG04		GND	SUM18	VLD18*	TRG04	GND				TRG04	T	GND			
10		GND		BCN0	SUM18*		GND	BCN0				GND		BCN0	T		
11	T	TRG05		GND	SUM17	VLD17*	TRG05	GND				TRG05	T	GND			
12		GND		ACCEPT	SUM17*		GND	ACCEPT				GND		ACCEPT	T		
13	T	TRG06		GND	SUM16	VLD16*	TRG06	GND				TRG06	T	GND			
14		GND		BANK	SUM16*		GND	BANK				GND		BANK	T		
15	T	TRG07		GND	SUM15	VLD15*	TRG07	GND				TRG07	T	GND			
16		GND		NOBUF*	SUM15*		GND	NOBUF*				GND		NOBUF*			
17	T	TRG08		GND	SUM14	VLD14*	TRG08	GND				TRG08	T	GND			
18		GND	T	RSV0	SUM14*		GND	RSV0				GND		RSV0	T		
19	T	TRG09		GND	SUM13	VLD13*	TRG09	GND				TRG09	T	GND			
20		GND	T	RSV1	SUM13*		GND	RSV1				GND		RSV1	T		
21	T	TRG10		GND	SUM12	VLD12*	TRG10	GND				TRG10	T	GND			
22		GND			SUM12*		GND					GND					
23	T	TRG11			SUM11	VLD11*	TRG11					TRG11	T				
24		GND			SUM11*		GND					GND					
25	T	TRG12			SUM10	VLD10*	TRG12					TRG12	T				
26		GND			SUM10*		GND					GND					
27	T	TRG13			SUM9	VLD9*	TRG13					TRG13	T				
28		GND			SUM9*		GND					GND					
29	T	TRG14			SUM8	VLD8*	TRG14		SUM8	VLD8*		TRG14	T			SUM21	VLD21*
30		GND			SUM8*		GND		SUM8*			GND				SUM21*	
31	T	TRG15					TRG15					TRG15	T				
32		GND					GND					GND					