# ZEUS Luminosity Monitor

# Memory Module

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# 1 General Remarks

- The Modules can only be used in a standard VME64 crate with an additional backplane DESY – FEA, board number 7254) installed.
- The set of 14 memory modules uses a VME address range of 128 MBytes.
- All VME accesses are long word accesses (**D32, D64**).
- All VME accesses use the extended address mode (**A32**).
- The VME base address for the set of 14 memory modules (bits 31...27) is fixed within a PAL and therefore not switchable. If not specified otherwise this base address is **0x20000000**.
  The next five bits (bits 26...22) are used to distinguish between the 14 modules. The values are depending on the module position within the crate and follow the geographical address scheme of the VME64 backplane.
- Power consumption: ~ 3 A @ 5 V and ~ 1.5 A @ 3.3 V.
- The version of the two XILINX chips can be read. The actual versions are
  SUM: **1**
  CONTROL: **2**

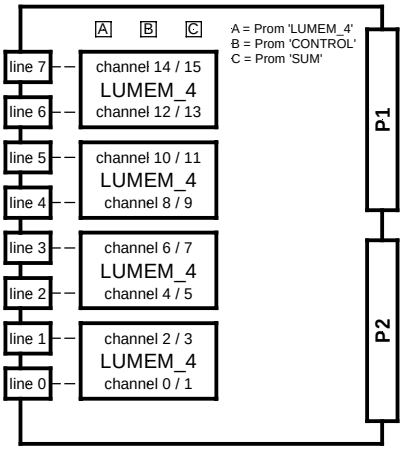
## *1.1 Data Files for Programmable Logic*

The latest versions of the data for the programmable logic chips can be found in the following files:

| | Chip | Position |
|---|---|---|
| VME configuration | ATMEL AT17E65 | FEA_VME_P1 |
| VME baseaddress | AMD PALCE22V10H-7JC/5 | U12 |
| fpga sum | ATMEL 17LV512 | UXSUM |
| fpga control | ATMEL 17LV512 | UXCON |
| fpga lumo-4 | ATMEL 17LV512 | UXMEZ |

## 1.2 Board Layout

The main board contains 4 mezzanine boards ('LUMEM_4'). Each of those mezzanine boards is connected to 2 input lines. Since two FADC channels are transmitted on each input line (time multiplexed), 4 channels are handled by each mezzanine board. The numbering of input lines and channels is the following:

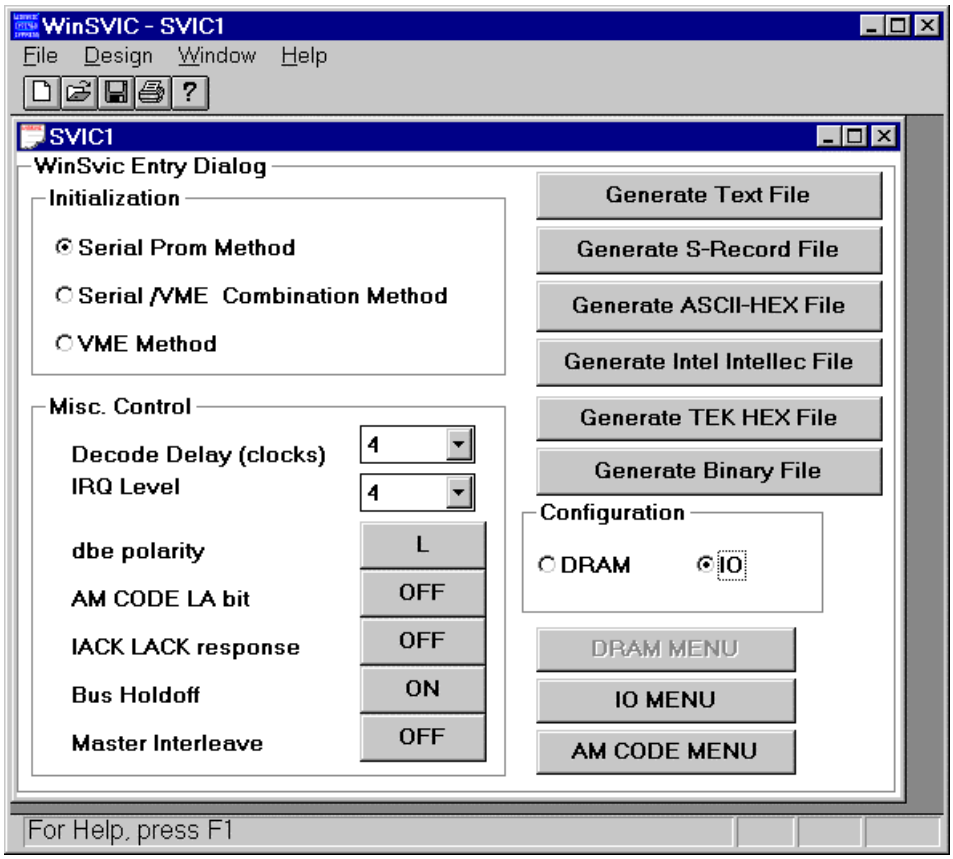


# 2 VME Interface

## *2.1 VME Interface Configuration*

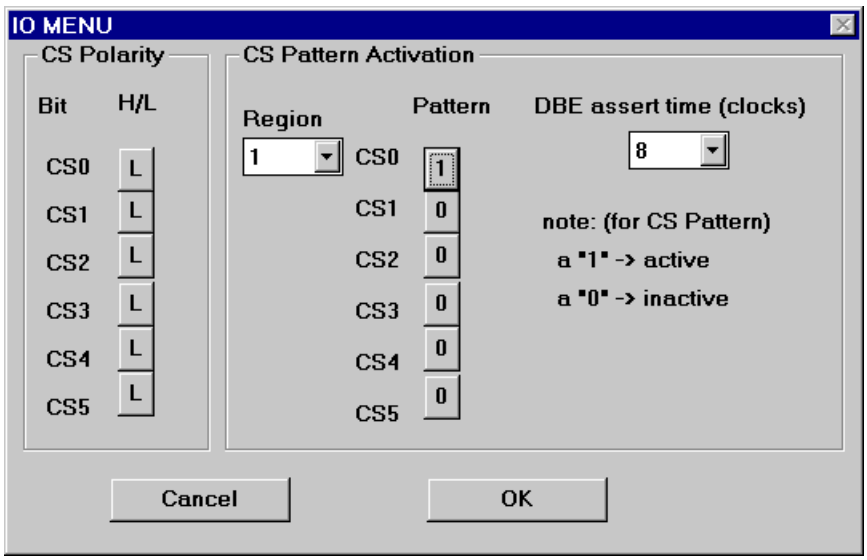
To access the VME bus the standard FEA mezzanine board 'FEA-VME-P1' is used. The modules have to be configured via a serial EEPROM ATMEL 'AT17E65' To generate the configuration data the program 'WinSVIC' (Cypress) has to be used.

### 2.1.1 Common Part

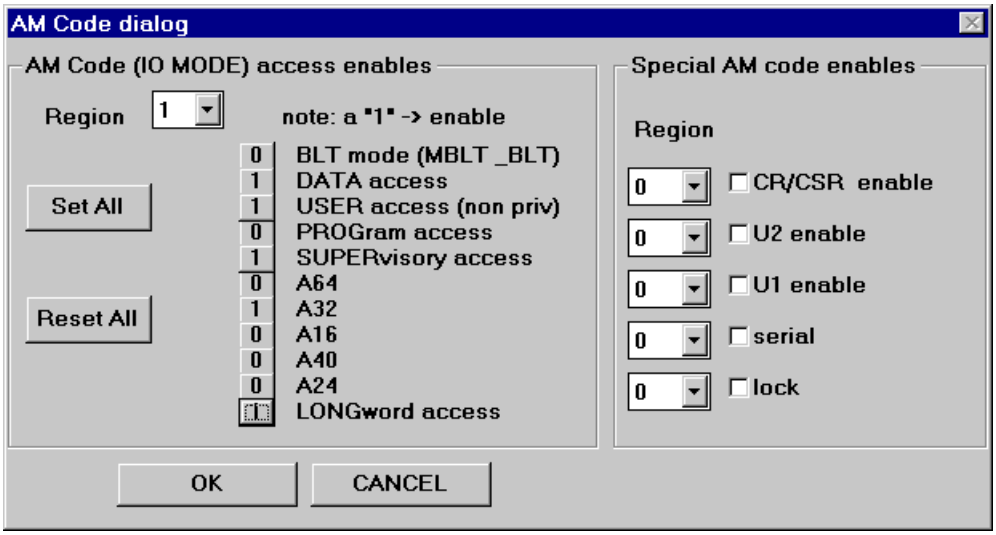


### 2.1.2 Control / Status Register Access

The Region 1 (input signal REG0) is used to access the control / status registers:

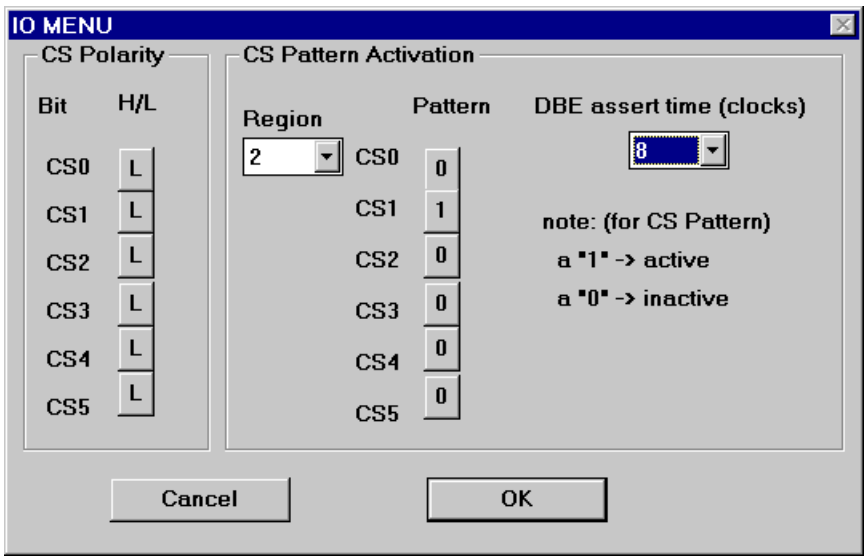



The control / status register access uses the A32 / D16 mode (AM codes '09' and '0D').
The A32 / D32 mode will work also (all addresses are longword aligned), but the upper 16 data bits will not be driven during readout:

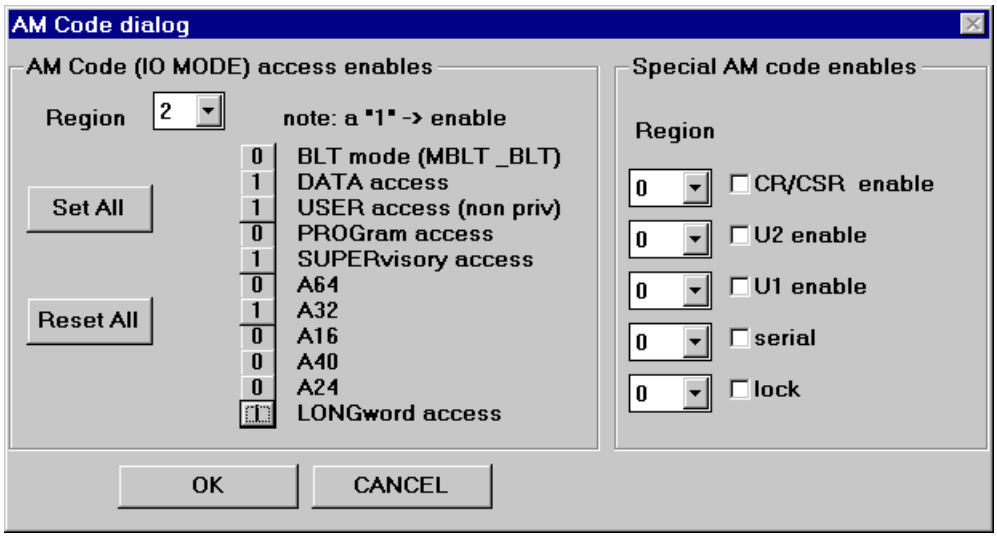


### 2.1.3 Lookup Table Access

The Region 2 (input signal REG1) is used to access the lookup tables:

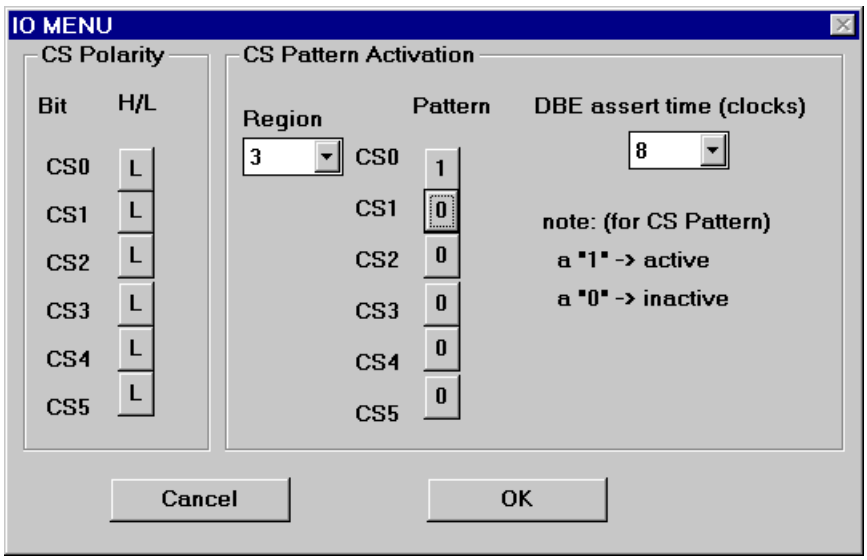



The lookup table access uses the A32 / D32 mode (AM codes '09' and '0D'):



### 2.1.4 Event Memory Access

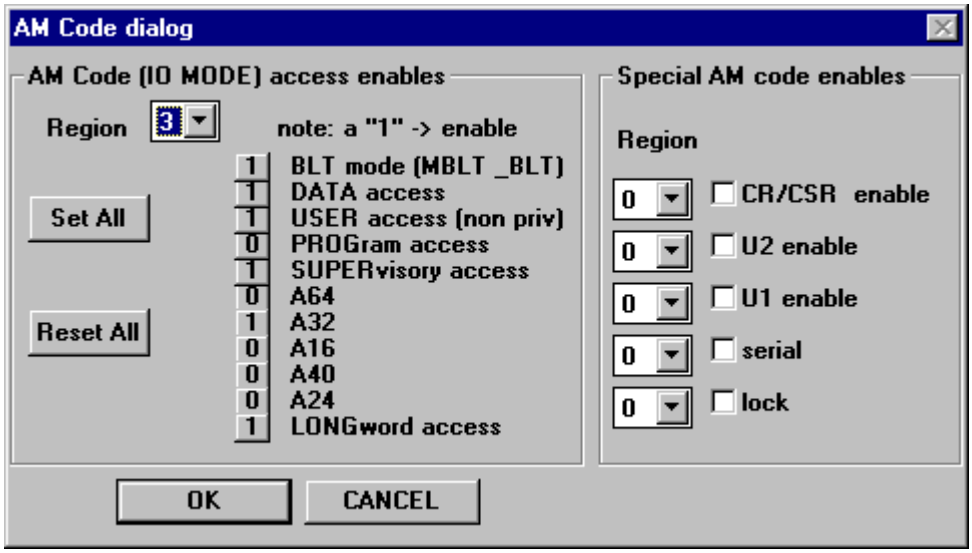
The Region 3 (input signal REG0 and REG1) is used to access the event memories:




The event memory access supports the following address modifiers:

'09', '0D' A32 / D32 data
'0B', '0F' A32 / D32 BLT
'08', '0C' A32 / D64 MBLT.

For the block modes the VME bus master has to guarantee that a new bus arbitration is executed only every 256 bytes (BLT) resp. 2048 bytes (MBLT). A new arbitration after the transfer of a smaller number of bytes will cause the loss of data words.



## *2.2 VME Addresses*

### 2.2.1 Memory Module Base Address

The VME base address ('**BA**') of a single memory module is defined by the leftmost 10 address bits. The bits 31...27 ('**BAMEM**') are common for all memory modules. They are defined in a PAL and therefore not switchable. The bits 26...22 are used to distinguish between the different memory modules and are give by the position within the crate.

| Crate Position | bits 26 25 24 23 22 | VME address (BAMEM+...) |
|---|---|---|
| **8** | 0 1 0 0 0 | 0x02000000 |
| **9** | 0 1 0 0 1 | 0x02400000 |
| **10** | 0 1 0 1 0 | 0x02800000 |
| **11** | 0 1 0 1 1 | 0x02C00000 |
| **12** | 0 1 1 0 0 | 0x03000000 |
| **13** | 0 1 1 0 1 | 0x03400000 |
| **14** | 0 1 1 1 0 | 0x03800000 |
| **15** | 0 1 1 1 1 | 0x03C00000 |
| **16** | 1 0 0 0 0 | 0x04000000 |
| **17** | 1 0 0 0 1 | 0x04400000 |
| **18** | 1 0 0 1 0 | 0x04800000 |
| **19** | 1 0 0 1 1 | 0x04C00000 |
| **20** | 1 0 1 0 0 | 0x05000000 |
| **21** | 1 0 1 0 1 | 0x05400000 |

### 2.2.2 Control / Status Register Access

Control / Status register accesses are executed if the VME base address 'BA' is correct and the address bits 21...20 are '00'; the address bits 19...5 are not decoded.
The recommended access mode is A32 / D16 (address bits 1...0 must be '00'). If the access mode A32 / D32 is used (which will work also) the upper two data bytes are not driven during read cycles (AM = 09, 0D).

| 31...22 | 21 | 20 | 19...5 | 4...2 | 1...0 | WRITE | READ | BITS |
|---|---|---|---|---|---|---|---|---|
| BA | 0 | 0 | . | 0 0 0 | 0 | reset | --- | 0 |
| BA | 0 | 0 | . | 0 0 1 | 0 | begin readout | --- | 0 |
| BA | 0 | 0 | . | 0 1 0 | 0 | end readout | --- | 1 |
| BA | 0 | 0 | . | 0 1 1 | 0 | sync fifo length (0..15) | --- | 5 |
| BA | 0 | 0 | . | 1 0 0 | 0 | delay fifo length (3..127) | --- | 7 |
| BA | 0 | 0 | . | 1 0 1 | 0 | command register | command register | 16 |
| BA | 0 | 0 | . | 1 1 0 | 0 | --- | status register 'EVT' | 16 |
| BA | 0 | 0 | . | 1 1 1 | 0 | --- | status register 'ERR' | 16 |

**BA:** VME base address for a single memory module (bits 31...22)
**'.':** don't care (not decoded)

**'END READOUT'**

with data bit 0 = 0: end readout local buffer, with data bit 0 = 1: end readout GFLT event

#### *2.2.2.1 Command Register Format*

| BITS | |
|---|---|
| **15...8** | Input Line Mask (7...0) |
| **7...6** | n.u. |
| **5...3** | Sum Window Control (if bit 1 = '1') |
| **2** | MODE: (reserved) |
| **1** | MODE: Sum Format |
| **0** | MODE: run |

**`Input Line Mask: 0:`** line enabled
**`1:`** line disabled
**`MODE 'Sum Format': 0:`** SUM (15...0) = total sum (truncated)
**`1:`** SUM (15...9) = total sum (12 bits), max channel (4 bits)
**`MODE 'run': 0:`** VME access to lookup table, no data taking
**`1:`** data taking, no VME access to lookup table

The input line mask bits diasble/enable both channels of the input line, i.e. bit 0 controls channnels 0 and 1, bit 1 channels 2 and 3, ..., bit 7 channels 14 and 15.

The format of the 'Total Sum' depends on the bits 'MODE: Sum Format' and 'Sum Window Control'. The originally calculated sum value ('SU', 21 bits) will be truncated according to the following scheme:

| MODE | WINDOWS | Total Sum | |
|---|---|---|---|
| | | **bits 15...4** | **bits 3...0** |
| **0** | **---** | SU(20...9) | SU(8...5) |
| **1** | **0** | SU(16...5) | max chan |
| **1** | **1** | SU(17...6) | max chan |
| **1** | **2** | SU(18...7) | max chan |
| **1** | **3** | SU(19...8) | max chan |
| **1** | **4** | SU(20...9) | max chan |

#### *2.2.2.2 Status Register 'EVT' Format*

The Status Register 'EVT' contains information related to the event buffer control.

| BITS | |
|---|---|
| **15...13** | n.u. |
| **12** | FLAG: error (see 'ERR' reg) |
| **11** | FLAG: GFLT event space avail. |
| **10** | FLAG: GFLT event avail. (read) |
| **9** | FLAG: write buffer available |
| **8** | FLAG: read buffer available |
| **7...0** | event count current read buffer |

#### *2.2.2.3 Status Register 'ERR' Format*

The Status Register 'ERR' contains version information and error flags.

| BITS | |
|---|---|
| **15...12** | XILINX 'SUM' version number |
| **11...8** | XILINX 'CONTROL' version number |
| **7** | n.u. |
| **6** | ERR: input line missing |
| **5** | ERR: SUM transfer out of sync |
| **4** | ERR: no space for GFLT event availa-ble |
| **3** | ERR: no local write buffer available |
| **2** | ERR: no GFLT event available for read |
| **1** | ERR: no local read buffer available |
| **0** | ERR: illegal lookup table access |

### 2.2.3 Lookup Table Access

Lookup Table accesses are executed if the VME base address 'BA' is correct and the address bits 21...20 are '01'. The access mode to be used is A32 / D32 (AM = 09, 0D).
The address has the following format:

| 31...22 | 21 | 20 | 19...17 | 16 | 15 | 14...2 | 1...0 |
|---|---|---|---|---|---|---|---|
| BA | 0 | 1 | input line | channel | LT / LTC | addr in LT | 0 |

**channel:** **0:** first channel on the input line
**1:** second channel on the input line
**LT / LTC:** **0:** main lookup table
**1:** correction lookup table

The correction lookup table value is added to the main lookup table value. Since both values and the result are handled as 17 bit signed numbers the user has to know (resp. guarantee) the following:

- all lookup table values are 17 bit signed integers in two's complement notation, i.e the lookup table values are numbers between –65536 and +65535
- generating the the sum of the main and the correction lookup table values the overflow bit will be dicarded, i.e. the sum must never exceed the range from –65536 to +65535
- the main lookup table values contain an additional 'zero' bit (bit 17); if this bit is set the value of this channel will not be included into the total sum.

### 2.2.4 Event Buffer Access

Event Buffer accesses are executed if the VME base address 'BA' is correct and the address bits 21...20 are '10'. The recommended access mode is A32 / D64 MBLT, but the standard A32 / D32 access mode will work also (AM = 08, 09, 0B, 0C, 0D, 0F). The event buffer can only be read.
The address has the following format:

| 31...22 | 21 | 20 | 19 | 18...2 | 1...0 | |
|---|---|---|---|---|---|---|
| BA | 1 | 0 | 0 | don't care | 0 | local event buffer |
| BA | 1 | 0 | 1 | don't care | 0 | GFLT event |

Since the event data have to be collected from different memories the bits 18...2 of the VME bus address will be ignored. The readout will always access the current read buffer (VME address bit 19 low) or the current GFLT event (VME address bit 19 high) , and the following command sequences have to be executed:

#### *2.2.4.1 Command Sequence for Reading a 'Local Event Buffer'*

- **Command: READ STATUS 'EVT'**
  find out if a read buffer is available and get the number of events stored in this buffer, starting the readout sequence if no buffer is available will cause an error condition
- **Command: BEGIN READOUT**
  this will initialize the current read buffer
- **Read the Event Buffer**
  the correct number of events should be read (MBLT mode or single word access)
- **Command: END READOUT (with data bit 0 = 0)**
  this will switch to the next read buffer

As long as the command 'END READOUT' has not been issued a re-read of the current read buffer can be initialized by a issuing the command 'BEGIN READOUT' again. Once the command 'END READOUT' has been issued the data of the currently handled read buffer are no longer available.

#### *2.2.4.2 Command Sequence for Reading a 'GFLT Event'*

- **Command: BEGIN READOUT**
  this will initialize the current event to be read in the GFLT event buffer
- **Read the Event**
  one event only can be read (MBLT mode or single word access), if more readout commands are given the same event will be read again
- **Command: END READOUT (with data bit 0 = 1)**
  this will switch to the next event to be read in the GFLT buffer

As long as the command 'END READOUT' has not been issued a re-read of the current event can be initialized by a issuing the command 'BEGIN READOUT' again. Once the command 'END READOUT' has been issued the data of the currently handled event are no longer available.

#### *2.2.4.3 Event Data Format*

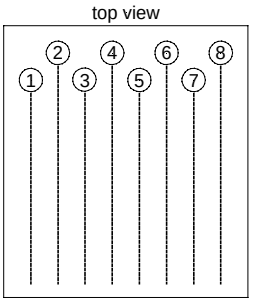
Each event consists of 40 bytes and has the following format (64 bit words):

| | 63...48 | 47...32 | 31...16 | 15...8 | 7...0 |
|---|---|---|---|---|---|
| **event header** | zero 14,12,10,8,6,4,2,0, sign 14,12,10,8,6,4,2,0 | sum | zero 15,13,11,9,7,5,3,1, sign 15,13,11,9,7,5,3,1 | bunch # | event size |
| **data word 0** | channel 0 | channel 2 | channel 4 | channel 6 | |
| **data word 1** | channel 8 | channel 10 | channel 12 | channel 14 | |
| **data word 2** | channel 1 | channel 3 | channel 5 | channel 7 | |
| **data word 3** | channel 9 | channel 11 | channel 13 | channel 15 | |

# 3 Front Panel Elements

## 3.1 Input Line Connectors

The eight input line connectors are standard 8 pin, shielded, category 5 'Modular Jacks' as they are used in high speed Ethernet systems (e.g.AMP-558342-1).




The (differential LVDS) input signals are terminated by 100 Ω resistors and received by an National Semiconductor 21-Bit Channel Link Receiver (DS90CR212, only the 16 low order bits are handled on the board), the shielding pins are connected to board ground. The connector pins are used as follows:

| Pin | Signal |
|---|---|
| 1 | A0M |
| 2 | A0P |
| 3 | A1M |
| 4 | A2M |
| 5 | A2P |
| 6 | A1P |
| 7 | CLKM |
| 8 | CLKP |

## 3.2 LEDs

There are 12 LEDs on the front panel. The 8 LEDs located between the input connectors indicate that a valid input signal is detected on the resp. input line (one serial telegram every 48 ns).
The 4 remaining LEDs are:

- **HC:** HERA clock (bunch crossing signal) detected at the backplane
- **BPV:** Serial sum transmission receiver synchronized
- **BNK:** 'BANK' signal detected at the backplane
- **ACC:** 'ACCEPT' signal detected at the backplane

# 4 Switches and Testpoints

## *4.1 Switches*

There are 10 switches on the board:

**JVLD –** leave the switch in the marked position

**JNOB –** connects the signal 'NOBUF*' to the backplane

**LDC01 –** 'on' if LUMEM_4 board 'UM01' is used as master
**MAS01 –** 'on' if LUMEM_4 board 'UM01' is used as master

**LDC23 –** 'on' if LUMEM_4 board 'UM23' is used as master
**MAS23 –** 'on' if LUMEM_4 board 'UM23' is used as master

**LDC45 –** 'on' if LUMEM_4 board 'UM45' is used as master
**MAS45 –** 'on' if LUMEM_4 board 'UM45' is used as master

**LDC67 –** 'on' if LUMEM_4 board 'UM67' is used as master
**MAS67 –** 'on' if LUMEM_4 board 'UM67' is used as master

**Attention:** **One** master only !!

## *4.2 Testpoints*

There are 14 testpoint on the main board and 3 testpoints on each LUMEM_4 bord:

**HC** - HERA bunch clock (96 ns)
**HC20** - HC * 2 (48 ns)
**HC20_** - HC * 2 inverted (48 ns)
**HC40** - HC * 4 (24 ns)
**BCN0** - Bunch Clock Number 0
**ACC** - ACCEPT (event trigger from backplane)
**GFLT** - First Level Trigger Event (from backplane)
**INCA** - INCREMENT Write Address (from backplane)
**BANK** - BANK (switch signal from backplane)
**NOBUF** - NOBUF (no write buffer available, to backplane)
**WEH1_** - WRITE Event Header First Word Enable
**WRAM_** - WRITE into Event Ram Pulse
**HCE_** - READ Event Header Enable
**HAD0** - READ Event Header Second Word Enable

**WRAM_** - WRITE into Event Ram Pulse
**DIA0** - Event Ram Input Bit 0, input line a
**DIB0** - Event Ram Input Bit 0, input line b

# 5 Backplane Connectors

## *5.1 Connector P1*

| | z | a | b | c | d |
|---|---|---|---|---|---|
| **1** | | D00 | BBSY* | D08 | |
| **2** | GND | D01 | BCLR* | D09 | |
| **3** | | D02 | ACFAIL* | D10 | |
| **4** | GND | D03 | BG0IN* | D11 | |
| **5** | | D04 | BG0OUT* | D12 | |
| **6** | GND | D05 | BG1IN* | D13 | |
| **7** | | D06 | BG1OUT* | D14 | |
| **8** | GND | D07 | BG2IN* | D15 | |
| **9** | | GND | BG2OUT* | GND | GAP* |
| **10** | GND | SYSCLK* | BG3IN* | SYSFAIL* | GA0* |
| **11** | | GND | BG3OUT* | BERR* | GA1* |
| **12** | GND | DS1* | BR0* | SYSRES* | +3.3V |
| **13** | | DS0* | BR1* | LWORD* | GA2* |
| **14** | GND | WRITE* | BR2* | AM5 | +3.3V |
| **15** | | GND | BR3* | A23 | GA3* |
| **16** | GND | DTACK* | AM0 | A22 | +3.3V |
| **17** | | GND | AM1 | A21 | GA4* |
| **18** | GND | AS* | AM2 | A20 | +3.3V |
| **19** | | GND | AM3 | A19 | |
| **20** | GND | IACK* | GND | A18 | +3.3V |
| **21** | | IACKIN* | SERA | A17 | |
| **22** | GND | IACKOUT* | SERB | A16 | +3.3V |
| **23** | | AM4 | GND | A15 | |
| **24** | GND | A07 | IRQ7* | A14 | +3.3V |
| **25** | | A06 | IRQ6* | A13 | |
| **26** | GND | A05 | IRQ5* | A12 | +3.3V |
| **27** | | A04 | IRQ4* | A11 | |
| **28** | GND | A03 | IRQ3* | A10 | +3.3V |
| **29** | | A02 | IRQ2* | A09 | |
| **30** | GND | A01 | IRQ1* | A08 | +3.3V |
| **31** | | -12V | +5STDBY | +12V | |
| **32** | GND | VCC | VCC | VCC | |

## 5.2 Connector P2

The Non-VME-Standard part of P2 (rows 'z', ‘a’, ‘c’, 'd') is used for the communication between the memory modules and the trigger module via the additional special backplane DESY-FEA 7254.

| | z | a | b | c | d |
|---|---|---|---|---|---|
| **1** | TRG00 | HC | VCC | | |
| **2** | GND | HC* | GND | | |
| **3** | TRG01 | (Hca) | | (SUM21) | (VALID21*) |
| **4** | GND | (Hca*) | A24 | (SUM21*) | GND |
| **5** | TRG02 | (HCb) | A25 | (SUM20) | (VALID20*) |
| **6** | GND | (HCb*) | A26 | (SUM20*) | GND |
| **7** | TRG03 | (HCc) | A27 | (SUM19) | (VALID19*) |
| **8** | GND | (HCc*) | A28 | (SUM19*) | GND |
| **9** | TRG04 | GND | A29 | (SUM18) | (VALID18*) |
| **10** | GND | BCN0 | A30 | (SUM18*) | GND |
| **11** | TRG05 | GND | A31 | (SUM17) | (VALID17*) |
| **12** | GND | ACCEPT | GND | (SUM17*) | GND |
| **13** | TRG06 | GND | VCC | (SUM16) | (VALID16*) |
| **14** | GND | BANK | D16 | (SUM16*) | GND |
| **15** | TRG07 | GND | D17 | (SUM15) | (VALID15*) |
| **16** | GND | NOBUF* | D18 | (SUM15*) | GND |
| **17** | TRG08 | GND | D19 | (SUM14) | (VALID14*) |
| **18** | GND | RSV0 | D20 | (SUM14*) | GND |
| **19** | TRG09 | GND | D21 | (SUM13) | (VALID13*) |
| **20** | GND | RSV1 | D22 | (SUM13*) | GND |
| **21** | TRG10 | GND | D23 | (SUM12) | (VALID12*) |
| **22** | GND | | GND | (SUM12*) | GND |
| **23** | TRG11 | | D24 | (SUM11) | (VALID11*) |
| **24** | GND | | D25 | (SUM11*) | GND |
| **25** | TRG12 | | D26 | (SUM10) | (VALID10*) |
| **26** | GND | | D27 | (SUM10*) | GND |
| **27** | TRG13 | | D28 | (SUM09) | (VALID09*) |
| **28** | GND | | D29 | (SUM09*) | GND |
| **29** | TRG14 | | D30 | SUM | VALID* |
| **30** | GND | | D31 | SUM* | GND |
| **31** | TRG15 | | GND | | |
| **32** | GND | | VCC | | |

The Trigger Specification Signals are currently used for:

- TRG00: GFLT event flag
- TRG01: INCA (increment the address within the GFLT buffer)
- TRG02: common reset

The signals 'TRG03' to 'TRG07' are not used, te signals 'TRG08' to 'TRG15' are not connected on the memory module.
The signals written in parenthesis are connected to these pins at slot positions 6 and 7 (trigger module) only. For details see the manual 'ZEUS Luminosity Monitor – Backplane'.

# 6 LUMEM_4 Mezzanine Boards Connectors

The connectors used are standard IEEE 1386 Board-to-Board 1.00mm Dual Row SMT connectors (e.g. AMP-120521-1 on the memory board, AMP-120525-1 on the mezzanine board).

## *6.1 Connector 'A' (JIN)*

| PIN | SIGNAL | | PIN | SIGNAL |
|---|---|---|---|---|
| **1** | ADCa(0) | | **2** | ADCCa |
| **3** | ADCa(1) | | **4** | GROUND |
| **5** | ADCa(2) | | **6** | GROUND |
| **7** | ADCa(3) | | **8** | GROUND |
| **9** | ADCa(4) | | **10** | GROUND |
| **11** | ADCa(5) | | **12** | GROUND |
| **13** | ADCa(6) | | **14** | GROUND |
| **15** | ADCa(7) | | **16** | GROUND |
| **17** | ADCa(8) | | **18** | GROUND |
| **19** | ADCa(9) | | **20** | GROUND |
| **21** | ADCa(10) | | **22** | GROUND |
| **23** | ADCa(11) | | **24** | GROUND |
| **25** | ADCa(12) | | **26** | GROUND |
| **27** | ADCa(13) | | **28** | ACTa* |
| **29** | ADCa(14) | | **30** | ACTb* |
| **31** | ADCa(15) | | **32** | GROUND |
| **33** | ADCb(0) | | **34** | ADCCb |
| **35** | ADCb(1) | | **36** | GROUND |
| **37** | ADCb(2) | | **38** | GROUND |
| **39** | ADCb(3) | | **40** | GROUND |
| **41** | ADCb(4) | | **42** | GROUND |
| **43** | ADCb(5) | | **44** | GROUND |
| **45** | ADCb(6) | | **46** | GROUND |
| **47** | ADCb(7) | | **48** | GROUND |
| **49** | ADCb(8) | | **50** | GROUND |
| **51** | ADCb(9) | | **52** | GROUND |
| **53** | ADCb(10) | | **54** | GROUND |
| **55** | ADCb(11) | | **56** | GROUND |
| **57** | ADCb(12) | | **58** | GROUND |
| **59** | ADCb(13) | | **60** | GROUND |
| **61** | ADCb(14) | | **62** | GROUND |
| **63** | ADCb(15) | | **64** | GROUND |

## *6.2 Connector 'B' (JVME)*

| PIN | SIGNAL | | PIN | SIGNAL |
|---|---|---|---|---|
| **1** | VMED(0) | | **2** | +3.3V |
| **3** | VMED(1) | | **4** | +3.3V |
| **5** | VMED(2) | | **6** | +3.3V |
| **7** | VMED(3) | | **8** | +3.3V |
| **9** | VMED(4) | | **10** | +3.3V |
| **11** | VMED(5) | | **12** | +3.3V |
| **13** | VMED(6) | | **14** | +3.3V |
| **15** | VMED(7) | | **16** | +3.3V |
| **17** | VMED(8) | | **18** | RSVBUS0 |
| **19** | VMED(9) | | **20** | RSVBUS1 |
| **21** | VMED(10) | | **22** | M_RUN |
| **23** | VMED(11) | | **24** | RESET (S) |
| **25** | VMED(12) | | **26** | RSVBUS2 |
| **27** | VMED(13) | | **28** | RSVBUS3 |
| **29** | VMED(14) | | **30** | GROUND |
| **31** | VMED(15) | | **32** | GROUND |
| **33** | VMED(16) | | **34** | GROUND |
| **35** | VMED(17) | | **36** | GROUND |
| **37** | VMEA(16) | | **38** | GROUND |
| **39** | VMEA(15) | | **40** | GROUND |
| **41** | VMEA(14) | | **42** | GROUND |
| **43** | VMEA(13) | | **44** | GROUND |
| **45** | VMEA(12) | | **46** | LTOE* |
| **47** | VMEA(11) | | **48** | LTWR* |
| **49** | VMEA(10) | | **50** | LTCEb* |
| **51** | VMEA(9) | | **52** | LTCEa* |
| **53** | VMEA(8) | | **54** | XIL_M0 |
| **55** | VMEA(7) | | **56** | XIL_CCLK |
| **57** | VMEA(6) | | **58** | XIL_DIN |
| **59** | VMEA(5) | | **60** | XIL_LDC* |
| **61** | VMEA(4) | | **62** | XIL_INIT* |
| **63** | VMEA(3) | | **64** | VMEA(2) |

## *6.3 Connector 'C' (JVAL)*

| PIN | SIGNAL | | PIN | SIGNAL |
|---|---|---|---|---|
| **1** | SUMa(0) | | **2** | SUMa(1) |
| **3** | GROUND | | **4** | SUMa(2) |
| **5** | HC20 | | **6** | SUMa(3) |
| **7** | GROUND | | **8** | SUMa(4) |
| **9** | HC20* | | **10** | SUMa(5) |
| **11** | GROUND | | **12** | SUMa(6) |
| **13** | +3.3V | | **14** | SUMa(7) |
| **15** | +3.3V | | **16** | SUMa(8) |
| **17** | +3.3V | | **18** | SUMa(9) |
| **19** | +3.3V | | **20** | SUMa(10) |
| **21** | +3.3V | | **22** | SUMa(11) |
| **23** | +3.3V | | **24** | SUMa(12) |
| **25** | +3.3V | | **26** | SUMa(13) |
| **27** | | | **28** | SUMa(14) |
| **29** | | | **30** | SUMa(15) |
| **31** | CWB(4) | | **32** | SUMa(16) |
| **33** | CWB(3) | | **34** | SUMb(0) |
| **35** | CWB(2) | | **36** | SUMb(1) |
| **37** | CWB(1) | | **38** | SUMb(2) |
| **39** | CWB(0) | | **40** | SUMb(3) |
| **41** | | | **42** | SUMb(4) |
| **43** | | | **44** | SUMb(5) |
| **45** | GROUND | | **46** | SUMb(6) |
| **47** | GROUND | | **48** | SUMb(7) |
| **49** | GROUND | | **50** | SUMb(8) |
| **51** | GROUND | | **52** | SUMb(9) |
| **53** | GROUND | | **54** | SUMb(10) |
| **55** | HC40 | | **56** | SUMb(11) |
| **57** | GROUND | | **58** | SUMb(12) |
| **59** | HC | | **60** | SUMb(13) |
| **61** | GROUND | | **62** | SUMb(14) |
| **63** | SUMb(16) | | **64** | SUMb(15) |

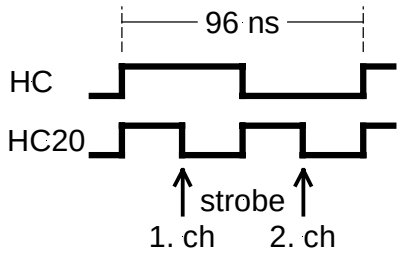
## *6.4 Connector 'D' (JDO')*

| PIN | SIGNAL | | PIN | SIGNAL |
|---|---|---|---|---|
| **1** | LFSL | | **2** | DOa(15) |
| **3** | LFDL | | **4** | DOa(14) |
| **5** | BANK | | **6** | DOa(13) |
| **7** | ACCEPT | | **8** | DOa(12) |
| **9** | | | **10** | DOa(11) |
| **11** | RAMCE* | | **12** | DOa(10) |
| **13** | CRB(4) | | **14** | DOa(9) |
| **15** | CRB(3) | | **16** | DOa(8) |
| **17** | CRB(2) | | **18** | DOa(7) |
| **19** | CRB(1) | | **20** | DOa(6) |
| **21** | CRB(0) | | **22** | DOa(5) |
| **23** | RAMAD(8) | | **24** | DOa(4) |
| **25** | ZOa | | **26** | DOa(3) |
| **27** | SOa | | **28** | DOa(2) |
| **29** | GFLT | | **30** | DOa(1) |
| **31** | ILMb | | **32** | DOa(0) |
| **33** | ILMa | | **34** | DOb(15) |
| **35** | ZOb | | **36** | DOb(14) |
| **37** | SOb | | **38** | DOb(13) |
| **39** | INCA | | **40** | DOb(12) |
| **41** | RAMAD(7) | | **42** | DOb(11) |
| **43** | RAMAD(6) | | **44** | DOb(10) |
| **45** | RAMAD(5) | | **46** | DOb(9) |
| **47** | RAMAD(4) | | **48** | DOb(8) |
| **49** | RAMAD(3) | | **50** | DOb(7) |
| **51** | RAMAD(2) | | **52** | DOb(6) |
| **53** | RAMAD(1) | | **54** | DOb(5) |
| **55** | RAMAD(0) | | **56** | DOb(4) |
| **57** | VCC (n.u.) | | **58** | DOb(3) |
| **59** | VCC (n.u.) | | **60** | DOb(2) |
| **61** | VCC (n.u.) | | **62** | DOb(1) |
| **63** | VCC (n.u.) | | **64** | DOb(0) |

# 7 Timing Specifications

## 7.1 Input Line Signals

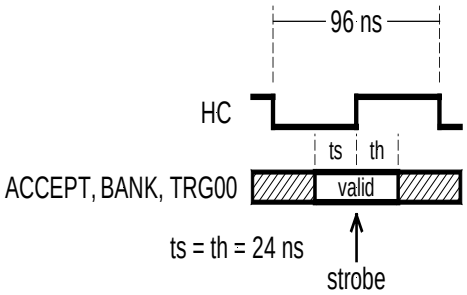
The information for two channels will be transmitted sequentially on each input line during each HERA bunch crossing period (96 ns). The serial data are transformed into a 16 bit parallel word (by the DS90CR212 chip) and stored into a 16 bit latch using the clock pulse delivered by the deserializer chip every 48 ns. This information then (after passing through the lookup table) will be synchronized with the HERA clock HC according to the following timing scheme:




Of the incoming data bits only the bits 13 ... 0 are used. Bits 12 ... 0 contain the data, bit 13 is used to discriminate between the two channels ('low' = 1. ch, 'high' = 2. ch). This additional bit is more or less the signal 'HC*' (but with the same timing as the other data bits).

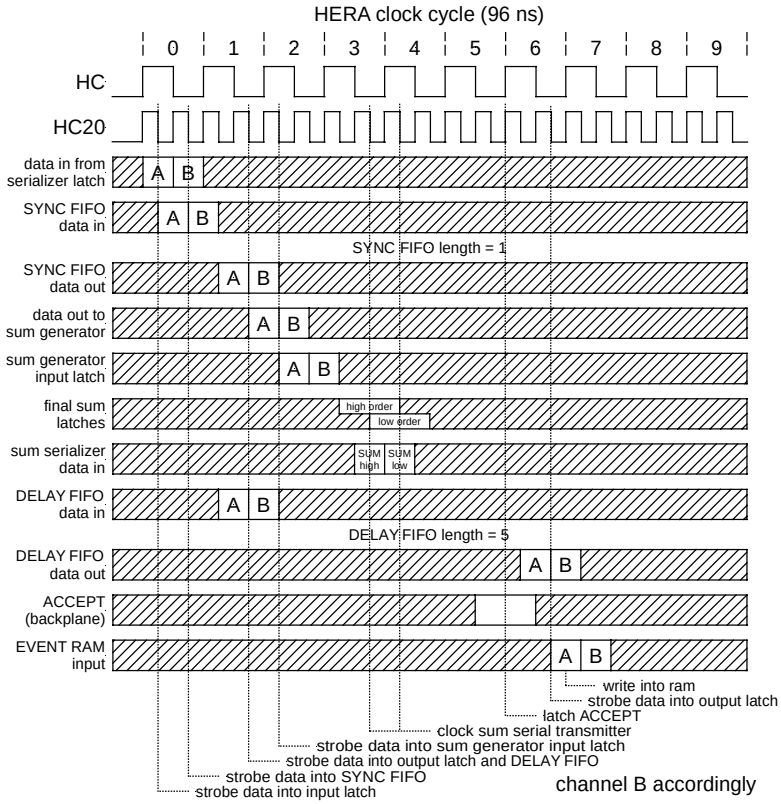
## 7.2 Backplane Signals

The three backplane signals 'ACCEPT', 'BANK', 'TRG00', 'TRG01' and 'TRG02' will be synchronized with the HERA clock 'HC' (strobed at the rising edge). The signals on the backplane should be valid according to the following timing scheme:



## *7.3 Data Flow Timing*

On their way through the module the data are delayed by two fifos.
The first fifo (SYNC FIFO) is used to synchronize the data in the different memory modules. The length of the SYNC FIFO can be set by a VME command, the legal range is 0 ... 15 (HERA clock cycles).
The second fifo (DELAY FIFO) is used to pipeline the data for the time needed by the trigger module to make a trigger decision. The length of the DELAY FIFO can also be set by a VME command, the legal range is 1 ... 63 (HERA clock cycles).
The following diagram shows the data flow through the module. The example shown is for a SYNC FIFO length of '1' and a DELAY FIFO length of '5'. The timing marks are given for channel 'A' only.



# 8 Event Data Storage

## *8.1 Event Types*

Every time an 'ACCEPT' signal is received the fifo output data will be transferred into the currently active event buffer. There are two different types of events, depending on the 'TRG00' signal:

- 'GFLT' events , generated by the global first level trigger (TRG00 = 1)
- 'LOCAL' events, generated by the trigger board (TRG00 = 0)

### 8.1.1 GFLT Events

There is one specific buffer for the GFLT events on the board, which can hold up to 256 events. This buffer is organized as an FIFO, there is no check against overflow or underflow.
To finally store an event in the buffer a signal 'INCA' (TRG02 = 1) has to be generated on the backplane. This will cause the switching of the address to the next free event location in the GFLT buffer. If the 'INCA' signal is missing the event will be ignored (overwritten by the next one).

### 8.1.2 LOCAL Events

The total available buffer space for the LOCAL events is divided into 30 buffers, each of those can hold up to 256 events.
Data will always be stored into the currently active 'write buffer'; there is **no** check for buffer overflow (access to the buffer will wrap around).
The signal 'BANK' on the backplane will cause the switch to the next write buffer. An event which occurs at the same time as the 'BANK' command will be stored into the old buffer. If a 'BANK' command occurs and no free write buffer is available an error flag will be set.
For the VME readout of the multiple buffers see section 2.2.4.

# 9 Revision History

- **17-Aug-00:** Revision 0
- **09-Apr-01:** Revision 2, Event storage algorithm changed
- **16-May-01:** Channel numbering and 'END READOUT' specification changed **( CONTROL -> 1, SUM -> 1)**
- **22-May-01:** Buffer organization corrected **( CONTROL -> 2)**