H1 Delay Module

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1 General Remarks

- The module is an 8-channel programmable delay line (range ~ 30 ... 1250 ns, resolution ~ 0.5 ns).
- For each channel one out of eight different data sources can be selected.
- The output pulse width is selectable for each channel (50 ns, 100 ns, 150 ns).
- The modules may be used in a standard 6U VME crate with only the P1 connector being connected. To utilize the full functionality a special H1 crate (5 row P2 connector) must be used.
- The modules uses a VME address range of 256 bytes.
- All VME accesses are word accesses (**D16**).
- All VME accesses use the standard address mode (**A24**).
- The VME base address of the module (bits 23...8) is selectable by four hexadecimal coded switches.
- Power consumption: ~ ? A @ 5 V and ~ ? A @ -12 V.
- The version of the XILINX chip can be read. The actual version is **3**.
- The version of the optional random trigger generator can be read. The actual version is **1**.

1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

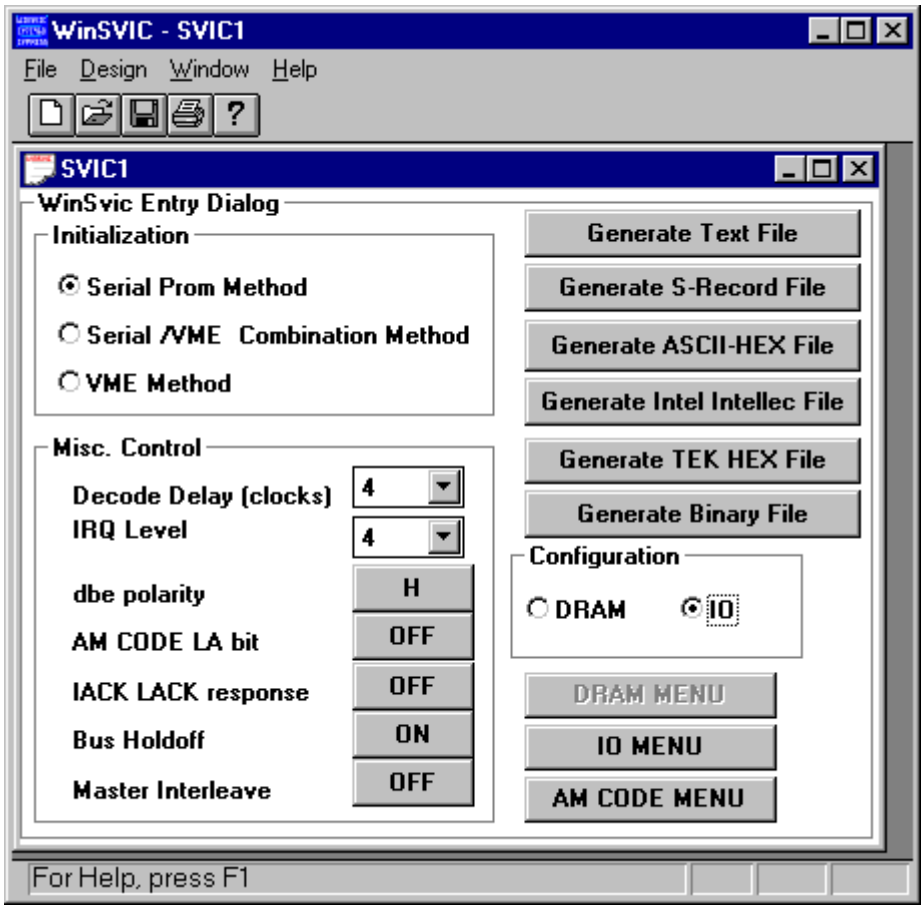
	Chip	Position
VME configuration	ATMEL AT17E65	FEA_VME_P1
fpga_delay	ATMEL AT17E256	U27

2 VME Interface

2.1 VME Interface Configuration

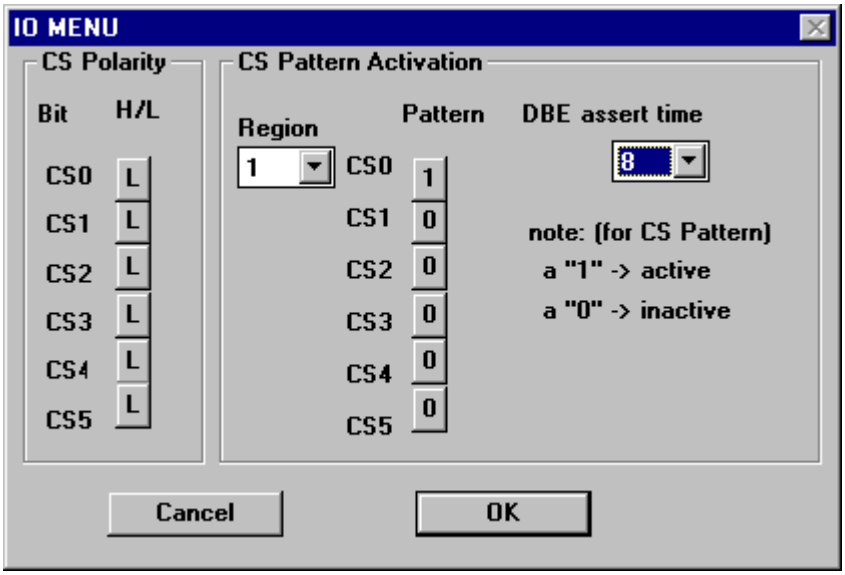
To access the VME bus the standard FEA mezzanine board 'FEA-VME-P1' is used. The modules have to be configured via a serial EEPROM ATMEL 'AT17E65' To generate the configuration data the program 'WinSVIC' (Cypress) has to be used.

2.1.1 Common Part

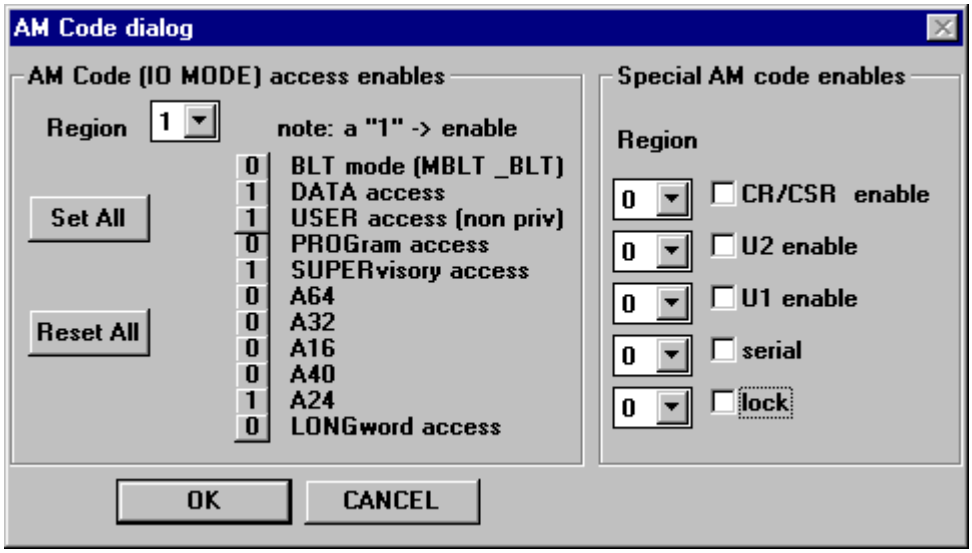


2.1.2 Control / Status Register Access

Only the region 1 (input signal REG0) is used to access the control / status registers:



The control / status register access uses the A24 / D16 mode (AM codes '39' and '3D').



2.2 VME Addresses

2.2.1 Memory Module Base Address

The VME base address ('**BA**', bits 23...8) of the board is defined by the 4 address switches:

SW4: bits 23...20
SW3: bits 19...16
SW2: bits 15...12
SW1: bits 11...8

2.2.2 Control / Status Registers

The supported access mode is A24 / D16 (address bit 0 must be '0').

23...8	7	6...4	3...1	0	WRITE	READ	BITS
BA	x	0 0 0	CHAN	0	mode	mode	16
BA	x	0 0 1	CHAN	0	delay	delay	16
BA	x	0 1 0	CHAN	0	hcdelay	hcdelay	8
BA	x	0 1 1	CHAN	0	reset counter	counter	0 / 16
BA	x	1 0 0	CHAN	0	VME trigger	serial number, version	0 / 8
BA	x	1 0 1	CHAN	0	counter reset mask	counter reset mask	8
BA	x	1 1 0	0 0 x	0	random generator 7..0	random generator 7..0	8
BA	x	1 1 0	0 1 x	0	random generator 15..8	random generator 15..8	8
BA	x	1 1 0	1 0 x	0	random generator 23..16	random generator 23..16	8
BA	x	1 1 0	1 1 x	0	random gen reset + rate	random generator version	1 / 8
BA	x	1 1 1	x x x	0	oscillator	oscillator	16

BA: VME base address (bits 23..8)
CHAN: output channel number

The Version number can be found in bits 4...0, the Module Serial Number in bits 7...5.

The Random Generator 'Rate Control Bit' will be set by the 'RESET' command (bit D0).
The 'Counter Reset Mask' defines which counter will be (asynchronously) forced to zero by a pulse on the front plate LEMO connector (bit n = channel n).

2.2.2.1 Mode Register Format

BITS	
15	n.u.
14..12	output line #
11	n.u.
10..8	input line #
7..4	n.u.
3	use HC delay (inp src = 2 only)
2..0	input source selector

`Input Source Selector: 7:` special input (active low signal on test point)
`6:` random trigger generator (active low)
`5:` oscillator
`4:` VME command (single pulse)
`3:` output line (bits 14..12)
`2:` input line (bits 10..8), synchronized with HC
`1:` input line (bits 10..8)
`0:` no output

2.2.2.2 Delay Register

15...8	7...0
delay (5 ns)	delay (0.5 ns)

This is the delay value used for the programmable delay lines. The actual delay value consists of this delay value plus a fixed value caused by the delay lines and the XILINX chip (~ 30 ns), which is differen for each channel and for each input source. To be able to calculate the exact value to be used the module has to be calibrated for each channel and each input source (i.e. 8 channels with 27 possible input sources each). In addition one has to measure the exact delay time for each of the 256 possible delay values of the 5ns delay line chip (for details see the 3D7408 datasheet).

2.2.2.3 HERA Clock Delay Register

15...8	7...0
n.u.	delay (number of HC's)

This value will only be used for Input Source Value = 2 and Mode Register Bit 3 = 1.

2.2.2.4 Counter

This counter contains the number of output pulses since the last reset for the selected output channel. A VME Write Command to this register will reset the counter.

2.2.2.5 VME Trigger

A VME Write Command to this register will generate one output pulse (if Input Source Value = 4).

2.2.2.6 Random Trigger Generator

Since the Random Trigger Generator is realized as a mezzanine board a whole lot of different data sources could be implemented. The version used on the actual board is a redesign of the H1 RanTrig2 used at the CTC Card (see H.Krehbiel: pAic RanTrig2 for the Fast CTC Card, 25.03.1997). The Random Trigger generator is used if Input Source Value = 6.

2.2.2.7 Oscillator

For Input Source Value = 5 a programmeble oscillator is used as data source (for all output channels). The value to be loaded is the oscillator frequency in 10 µs units, i.e. the possible frequency range is 100 KHz to ~ 2 Hz.

3 Front Panel Elements

3.1 Input Line Connectors

The ten input connectors (JI0...JI7, JHC, JRSV) are standard LEMO Connectors (DESY 26217). The input signals are NIM signals, the active polarity of the input signals JI0...JI7 can be selected by jumpers (JMI0...JMI7).

3.2 Output Line Connctors

The eight ouput connectors (JO0...JO7) are standard LEMO Connectors (DESY 26217). The output signals are NIM signals.

3.3 LEDs

There are 3 LEDs on the front panel for each of the eight channels:

- **green:** Input Line Signal
- **yellow:** Output Line Signal
- **red:** 'DANGER', the input line signal occurs within ~ ± 12 ns of the rising edge of the HERA clock (for Input Source Value = 2 only)

The green 'Input Line Signal' led will be on permanently if the input line polarity is set to 'active low' and there is no signal on the input connector.

There are two LEDs on the front panel to signal VME accesses:

- **green:** VME Write Access (WR)
- **red** VME Read Access (RD)

4 Switches and Testpoints

4.1 Switches

There are 45 switches on the board:

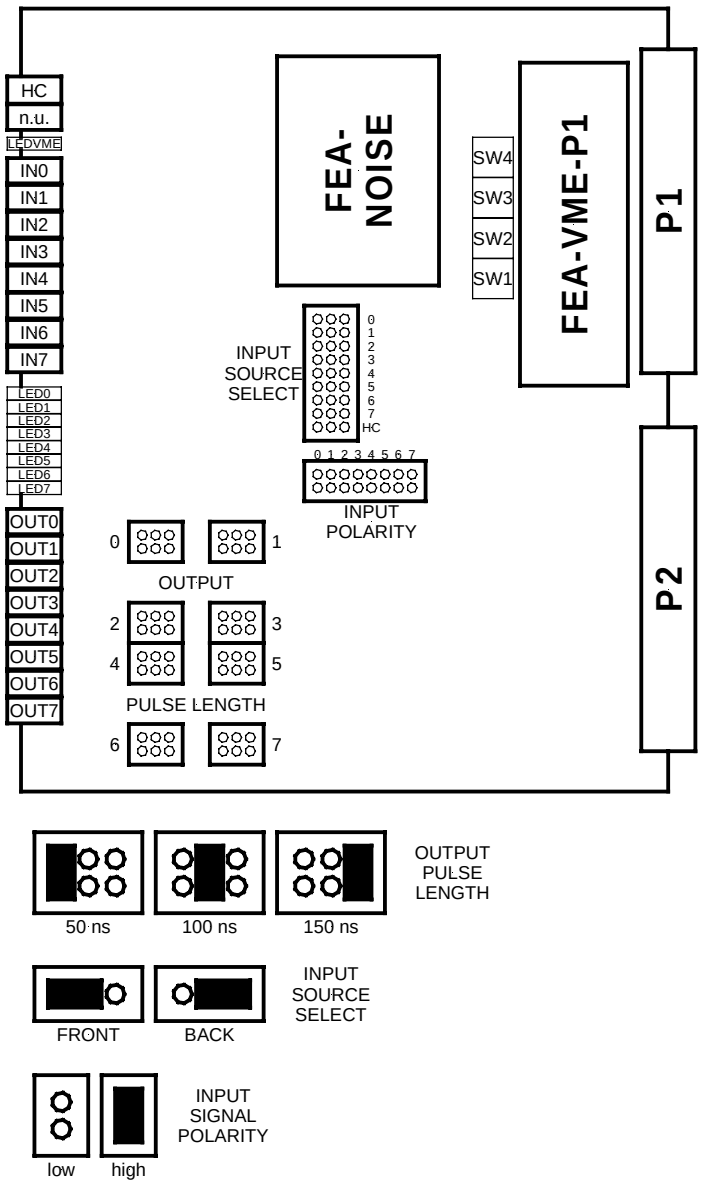
SW4 – VME base address bits 20...23
SW3 – VME base address bits 16...21
SW2 – VME base address bits 12...15
SW1 – VME base address bits 08...11

JMHC – front / back selector HERA clock (HC)
JMI0...JMI7 – front / back selector input line 0...7

JS0...JS7 – polarity selector input line 0...7 ('on' = active high)

Jn1 – `'on':` output pulse length channel '**n**' (n = 0...7) = 50 ns
Jn2 – `'on':` output pulse length channel '**n**' (n = 0...7) = 100 ns
Jn3 – `'on':` output pulse length channel '**n**' (n = 0...7) = 150 ns
(one only for each channel)

Board Layout and Switch Positions:



5 Backplane Connectors

5.1 Connector P1

	a	b	c
1	D00	*(BBSY*)*	D08
2	D01	*(BCLR*)*	D09
3	D02	*(ACFAIL*)*	D10
4	D03	*(BG0IN*)*	D11
5	D04	*(BG0OUT*)*	D12
6	D05	*(BG1IN*)*	D13
7	D06	*(BG1OUT*)*	D14
8	D07	*(BG2IN*)*	D15
9	GND	*(BG2OUT*)*	GND
10	*(SYSCLK*)*	*(BG3IN*)*	*(SYSFAIL*)*
11	GND	*(BG3OUT*)*	*(BERR*)*
12	DS1*	*(BR0*)*	*SYSRES**
13	DS0*	*(BR1*)*	LWORD*
14	WRITE*	*(BR2*)*	AM5
15	GND	*(BR3*)*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	*(SERA)*	A17
22	IACKOUT*	*(SERB)*	A16
23	AM4	GND	A15
24	A07	*(IRQ7*)*	A14
25	A06	*(IRQ6*)*	A13
26	A05	*(IRQ5*)*	A12
27	A04	*(IRQ4*)*	A11
28	A03	*(IRQ3*)*	A10
29	A02	*(IRQ2*)*	A09
30	A01	*(IRQ1*)*	A08
31	-12V	*(+5STDBY)*	*(+12V)*
32	VCC	VCC	VCC

5.2 Connector P2

The (optional) connector P2 is a five row connector as it is used in the H1 trigger crates.(rows ‘a’, ‘c’, 'd') is used for the communication between the memory modules and the trigger module via the additional special backplane DESY-FEA 7254.

	a	b	(c)	d	e
1	VCC			VCC	VCC
2				IN0	IN0*
3				IN1	IN1*
4				IN2	IN2*
5				IN3	IN3*
6	GND			IN4	IN4*
7	GND			IN5	IN5*
8	GND			IN6	IN6*
9	GND			IN7	IN7*
10	GND				
11					
12					
13				HC	HC*
14					
15					
16					
17					
18					
19					
20					
21					
22					
23				OUT0	OUT0*
24				OUT1	OUT1*
25				OUT2	OUT2*
26				OUT3	OUT3*
27				OUT4	OUT4*
28				OUT5	OUT5*
29				OUT6	OUT6*
30				OUT7	OUT7*
31	GND			GND	GND
32	-5,2V			-5,2V	-5,2V

The differential input signals (HC, IN0...IN7) follow the H1 standard (received by a MC100325 receiver).
The differential output signals (OUT0...OUT7) follow the H1 standard (driven by a SN75110 driver).

6 Revision History

- **30-Jul-01:** Revision 0
- **24-Oct-01:** VME addressing changed to 16-bit data words
- **31-Oct-01:** Counter reset under mask via front plate LEMO connector added (**VERSION: 2**)
- **20-Nov-01:** Module Serial Number added (**VERSION: 3**)