HERAB Fast Control System

Daughter Module

Author: Gerd Hochweller, Peter Gasiorek

1 GENERAL REMARKS

1.1 DATA FILES FOR PROGRAMMABLE LOGIC

2 CLUSTER/CRATE ADDRESS CODE CONNECTOR (JCOD)

3 FIBER DATA INPUT CONNECTOR (JINP)

3.1 FIBER LINK DATA FORMAT
3.2 DAUGHTER COMMAND CODES

4 DIAGNOSTIC CONNECTOR (DIAG)

5 CAN BUS

5.1 CAN BUS CONNECTORS (CAN1, CAN2)
5.2 CAN CHIP RESET SELECTOR
5.3 CAN BUS CONTROLLER DATA FORMAT
5.4 CAN BUS DATA FORMATS
5.4.1 CAN Bus 'Command' Data
5.4.2 CAN Bus 'Read' Data

6 BACKPLANE CONNECTOR (P2)

6.1 JUMPER
6.2 TRIGGER CODES (BACKPLANE)

7 REVISION HISTORY

1 General Remarks

- The module uses one slot in the crate.
- The module is available in two different board sizes:
  standard (160 mm), actual board number: 6339-5 (modified 6339-4 ok)
  long (220 mm), actual board number: 6729-1 (modified 6729-0 ok)
- For the cluster/crate addressing a special code connector is used on the board, the actual values of the cluster and crate addresses are visible on the front panel.
- The version numbers of the CAN controller program and the XILINX chip can be read. The actual versions are
  CAN: **9**
  XIL: **2**
- Power consumption: ~ 0.6 A @ 5 V

1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

	Chip	Position	
CAN controller	ATMEL 17E65	U5	(call G.Bialek, FEB)
fpga logic	ATMEL 17E128	U25	

2 Cluster/Crate Address Code Connector (JCOD)

The JCOD-Connector is a modified 16-pin dip socket connector. The encoding of the Cluster- and Crate-Address is achieved by cutting off some of the pins (pin missing = 1).

Pin	Signal
1	GND
2	DAUGHTER(4)
3	DAUGHTER(2)
4	DAUGHTER(0)
5	CLUSTER(4)
6	CLUSTER(2)
7	CLUSTER(0)
8	GND
9	GND
10	CLUSTER(1)
11	CLUSTER(3)
12	CLUSTER(5)
13	DAUGHTER(1)
14	DAUGHTER(3)
15	DAUGHTER(5)
16	GND

3 Fiber Data Input Connector (JINP)

The JINP connector is a standard 2*30 pin 'Low Profile Header' (e.g. 3M-3597-5002).
The (differential) input signals are terminated by 100 Ω resistors and received by differential line receivers DS90C032.
The differential signals use positive true logic, i.e. the signal is 'true' if SIG 0 'high', SIG* = 'low'.

Pin	Signal		Pin	Signal
1	GND		2	GND
3	FIBER(0)		4	FIBER*(0)
5	FIBER(1)		6	FIBER*(1)
7	FIBER(2)		8	FIBER*(2)
9	FIBER(3)		10	FIBER*(3)
11	GND		12	GND
13	FIBER(4)		14	FIBER*(4)
15	FIBER(5)		16	FIBER*(5)
17	FIBER(6)		18	FIBER*(6)
19	FIBER(7)		20	FIBER*(7)
21	GND		22	GND
23	FIBER(8)		24	FIBER*(8)
25	FIBER(9)		26	FIBER*(9)
27	FIBER(10)		28	FIBER*(10)
29	FIBER(11)		30	FIBER*(11)
31	GND		32	GND
33	FIBER(12)		34	FIBER*(12)
35	FIBER(13)		36	FIBER*(13)
37	FIBER(14)		38	FIBER*(14)
39	FIBER(15)		40	FIBER*(15)
41	GND		42	GND
43	FIBER(16)		44	FIBER*(16)
45	FIBER(17)		46	FIBER*(17)
47	FIBER(18)		48	FIBER*(18)
49	FIBER(19)		50	FIBER*(19)
51	CMD AV (n.u.)		52	CMD AV* (n.u.)
53	LINK READY		54	LINK READY*
55	ERROR		56	ERROR*
57	STROBE		58	STROBE*
59	ENABLE		60	ENABLE

3.1 Fiber Link Data Format

The 20-bit fiber link data words have the following format:

	19 ... 16	15 ... 8	7 ... 0
FLT EVENT	1 0 0 0	0 0 0 0 0 0 0 0	FLT-BX #
RANDOM TRG	1 0 0 1	0 0 0 0 0 0 0 0	FLT-BX #
VME TRG	1 0 1 0	0 0 0 0 0 0 0 0	FLT-BX #
LEMO1 TRG	1 1 0 0	0 0 0 0 0 0 0 0	FLT-BX #
LEMO2 TRG	1 1 0 1	0 0 0 0 0 0 0 0	FLT-BX #
LEMO3 TRG	1 1 1 0	0 0 0 0 0 0 0 0	FLT-BX #
LEMO4 TRG	1 1 1 1	0 0 0 0 0 0 0 0	FLT-BX #
COMMAND HIGH	0 1 1 0	0 0 0 0 0 A A A	DATA
COMMAND LOW	0 1 1 1	0 0 D D D D D D	0 0 C C C C C C
FLT #	0 1 0 1	FLT #	
BX #	0 0 0 0	0 0 0 0 0 0 0 0	BX #

A: command code
D: daughter number
C: cluster number

3.2 Daughter Command Codes

Daughter command codes and related data ('TP' = 'test pulse'):

COMMAND CODE	COMMAND	DATA
0	latch and reset FLT count (CAN)	---
1	issue TP	TP delay(0...255)
2	load strobe pattern	strobe pattern (0...255)
3	toggle strobe	toggle pattern (0...255)
4	load BX delay	BX delay(0...255*.5ns)
5	load BX offset	BX offset (0...7)
6	load trigger mask	trigger mask (0...255)
7	load TP trigger data	TP data

trigger mask: **X'80':** hardware trigger (LEMO 4)
X'40': hardware trigger (LEMO 3)
X'20': hardware trigger (LEMO 2)
X'10': hardware trigger (LEMO 1)
X'08': TP trigger
X'04': software trigger (VME)
X'02': random trigger
X'01': FLT accept trigger

TP data: **X'80':** disable test pulse backplane
X'40': disable test pulse frontplane
X'20': enable automatic test pulse generation (at (BX modulo 32) = 0)
X'10': enable (and start) fiber transfer test mode
X'08': \
X'04': \ TP Trigger BX Offset
X'02': / (0...15 * 96 ns)
X'01': /

If the TP trigger BX offset is zero no test pulse will be generated.
In fiber transfer test mode a continuous check of the BX-number is executed. If an error occurs the 'Fiber Error Flag' will be set.

4 Diagnostic Connector (DIAG)

The DIAG connector is a standard 2*17 pin 'Low Profile Header' (e.g. 3M-3594-5002).
The (differential) output signals are driven by differential line drivers AM26LS31.
The differential signals use positive true logic, i.e. the signal is 'true' if SIG 0 'high', SIG* = 'low'.

Pin	Signal		Pin	Signal
1	GND		2	GND
3	BX-PULSE (del.)		4	BX-PULSE* (del.)
5	TEST-PULSE		6	TEST-PULSE*
7	TEST-PULSE		8	TEST-PULSE*
9	TEST-PULSE		10	TEST-PULSE*
11	TEST-PULSE		12	TEST-PULSE*
13	GND		14	GND
15	RESET		16	RESET*
17	STROBE1		18	STROBE1*
19	STROBE2		20	STROBE2*
21	STROBE3		22	STROBE3*
23	STROBE4		24	STROBE4*
25	STROBE5		26	STROBE5*
27	STROBE6		28	STROBE6*
29	STROBE7		30	STROBE7*
31	FLTACC		32	FLTACC*
33	GND		34	GND

5 CAN Bus

The CAN bus interface allows access to some of the board register values for diagnostic purpose.

5.1 CAN Bus Connectors (CAN1, CAN2)

The CAN1 and CAN2 connectors are standard 4-position 'Low Profile Modular Jacks' (e.g. AMP-215875-3).
The respective pins of both connectors are directly connected, i.e. there is no preferred input or output connector.

Pin	Signal
1	CAN
2	CAN*
3	SIG
4	SIG*

The signal 'SIG' may be used for resetting the interface or similar functions.

5.2 CAN Chip Reset Selector

There are two possibilities to reset and initialize the CAN controller chip:

- JMP1 = 'CAN': the signal 'SIG' on the CAN bus connector is used as the reset signal
- JMP1 = 'XIL': the XILINX chip 'READY' signal is used as the reset signal

The position 'XIL' should be used in the current version.

5.3 Can Bus Controller Data Format

The CAN bus controller generates 4 bits of output data and receives 8 bits of input data. Three of the four output data bits are used to select the information on the input data lines.

CAN data out 3 2 1 0	function	CAN data in
0 0 0 0	sel data in	FLT count bits 7..0
0 0 0 1	sel data in	FLT count bits 15..8
0 0 1 0	sel data in	FLT count bits 23..16
0 0 1 1	sel data in	FLT count bits 31..24
0 1 0 0	sel data in	strobe bit pattern
0 1 0 1	sel data in	trigger mask
0 1 1 0	sel data in	control info 1
0 1 1 1	sel data in	control info 2
1 0 0 0	sel data in	XILINX version
1 1 1 1	reset flags	---

	control info 1:	**control info 2:**
X'80':	daughter address bit 3	cluster address bit 5
X'40':	daughter address bit 2	cluster address bit 4
X'20':	daughter address bit 1	cluster address bit 3
X'10':	daughter address bit 0	cluster address bit 2
X'08':	0	cluster address bit 1
X'04':	fiber error flag	cluster address bit 0
X'02':	test pulse issued flag	daughter address bit 5
X'01':	reset pulse issued flag	daughter address bit 4

The 'fiber error flag' indicates one of two possible error conditions:

- fiber receiver hardware error (reset by CAN command 'reset flags')
- wrong BX-number detected in 'fiber transfer test mode' (reset each time the test mode is switched on)

5.4 CAN Bus Data Formats

5.4.1 CAN Bus 'Command' Data

11 ID bits and 24 data bits (bytes 1...3) are transferred via tha CAN bus lines from the CAN bus master to the daughter modules.
The 11 ID bits must be all '0'.
The 3 data bytes must contain the following information:

byte	data
1	0 0 C C C C C C
2	0 0 D D D D D D
3	Q M 0 R R R R R

C: cluster address (C = 0: all clusters)
D: daughter address (D = 0: all daughters)
Q: **0:** configuration command
- **M:** **0:** free running mode
  - **R:** data transfer rate (every 'R' * 250 ms)
- **1:** single data request mode
  - **R:** n.u.

1: single data request command
- **M:** n.u.
- **R:** n.u.

5.4.2 CAN Bus 'Read' Data

64 data bits are transferred via the CAN bus lines (bit 63 transferred first) from the daughter module to the CAN bus master.

bits	data
63 ... 32	FLT count (32)
31 ... 24	strobe bit pattern (8)
23 ... 16	trigger mask (8)
15 ... 11	CAN version
10	fiber error flag
9	test pulse issued flag
8	reset pulse issued flag
7 ... 0	XILINX version

6 Backplane Connector (P2)

The unipolar signals are driven by bus drivers 74ABT574 or 74ABT240, the differential signals are driven by differential line drivers AM26LS31.

	a	c
1	VCC	GND
2	TEST-PULSE	TEST-PULSE*
3	GND	GND
4	TCOD(0)	TCOD(1)
5	ERROR	TCOD(2)
6	FLT-ACCEPT	BX-FLT(0)
7	BX-FLT(1)	BX-FLT(2)
8	BX-FLT(3)	BX-FLT(4)
9	BX-FLT(5)	BX-FLT(6)
10	FLT(0)	FLT(1)
11	FLT(2)	FLT(3)
12	FLT(4)	FLT(5)
13	FLT(6)	FLT(7)
14	FLT(8)	FLT(9)
15	FLT(10)	FLT(11)
16	FLT(12)	FLT(13)
17	FLT(14)	FLT(15)
18	GND	GND
19	BX(0)	BX(1)
20	BX(2)	BX(3)
21	BX(4)	BX(5)
22	BX(6)	BX(7)
23	GND	GND
24	RESET	STROBE1
25	STROBE2	STROBE3
26	STROBE4	STROBE5
27	STROBE6	STROBE7
28	GND	GND
29	SIG2	SIG1
30	GND	GND
31	BX-CLOCK	BX_CLOCK*
32	VCC	GND

6.1 Jumper

JMP2: FLT-ACCEPT mode selection (level or pulse)

JMP3: drive the LEMO input signal SIG2 (pullup 4.7 kΩ to VCC) onto the backplane

JMP4: drive the LEMO input signal SIG1 (pullup 4.7 kΩ to VCC) onto the backplane

6.2 Trigger Codes (Backplane)

c5 c4 a4	Event Type	backplane BX-FLT info
0 0 0	FLT-ACCEPT trigger	FLT-BX #
0 0 1	random trigger	BX # - LATACC
0 1 0	software trigger (VME)	BX # - LATACC
0 1 1	test pulse trigger	actual BX #
1 0 0	hardware trigger (LEMO 1)	BX # - LATACC
1 0 1	hardware trigger (LEMO 2)	BX # - LATACC
1 1 0	hardware trigger (LEMO 3)	BX # - LATACC
1 1 1	hardware trigger (LEMO 4)	BX # - LATACC

FLT-BX #: BX # from first level trigger (Master Module)
LATACC : content of 'Latest Accept'-register (Master Module)

7 Revision History

- **27-Jul-98:** Revision 4
- **14-Sep-98:** trigger mask description corrected
- **10-Feb-99:** Revision 5
- **08-Jun-99:** automatic test pulse generation feature added
- **14-Jul-99:** BX value test mode feature added
  XILINX version control added, -> **'CAN' version 9, 'XIL' version 2**
- **27-Oct-00:** manual changed (CAN command format description added)