HERAB Fast Control System

Master Module

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1 General Remarks

- The module requires a VME address range of 2048 bytes.
- All VME accesses are long word accesses (**D32**).
- All VME accesses use the standard address mode (**A24**).
- The VME base address (bits 23...11) is fixed within a PAL and therefore not switchable.
  If not specified otherwise the base address is **0x010000**.
- There is no arbitration between the incrementation and the readout of the statistics and histogram counters. If the hardware logic generates an incrementation command during the VME readout cycle the readout result is unpredictable.
- Writing (via VME) into the histogram memory should only be used for testing and resetting the memory. Write commands during run time may cause unpredictable results.
- The control registers are readable via VME. When reading a short (8-bit) register the unused bits (31...9) are forced to zero by the hardware.
- To obtain a correct result in reading the BX-TAG counter the high order part must be handled first.
- The module uses two slots in the VME crate.
- Power consumption: ~ 1.2 A @ 5 V.
- The XILINX chip XC4025E at U18 contains only the statistics counters, the histogram memory, the BX-TAG counter and the complete SHARC link control. The chip is **not** necessary for the basic features of the fast control system and may be omitted in the test setup versions of the module for cost reasons.
- The version of the two XILINX chips can be read. The actual versions are
  LOGIC: **9**
  STATISTICS (if supported): **4**
- To minimize distorsions in the distribution of the BX pulse a separate differential driver for each fiber transmitter module is used. To easily distribute these point-to-point signals together with the bus signals a special mezzanine backplane has been developed (board number FEA 6812).

1.1 Data Files for Programmable Logic

The latest versions of the data for the programmable logic chips can be found in the following files:

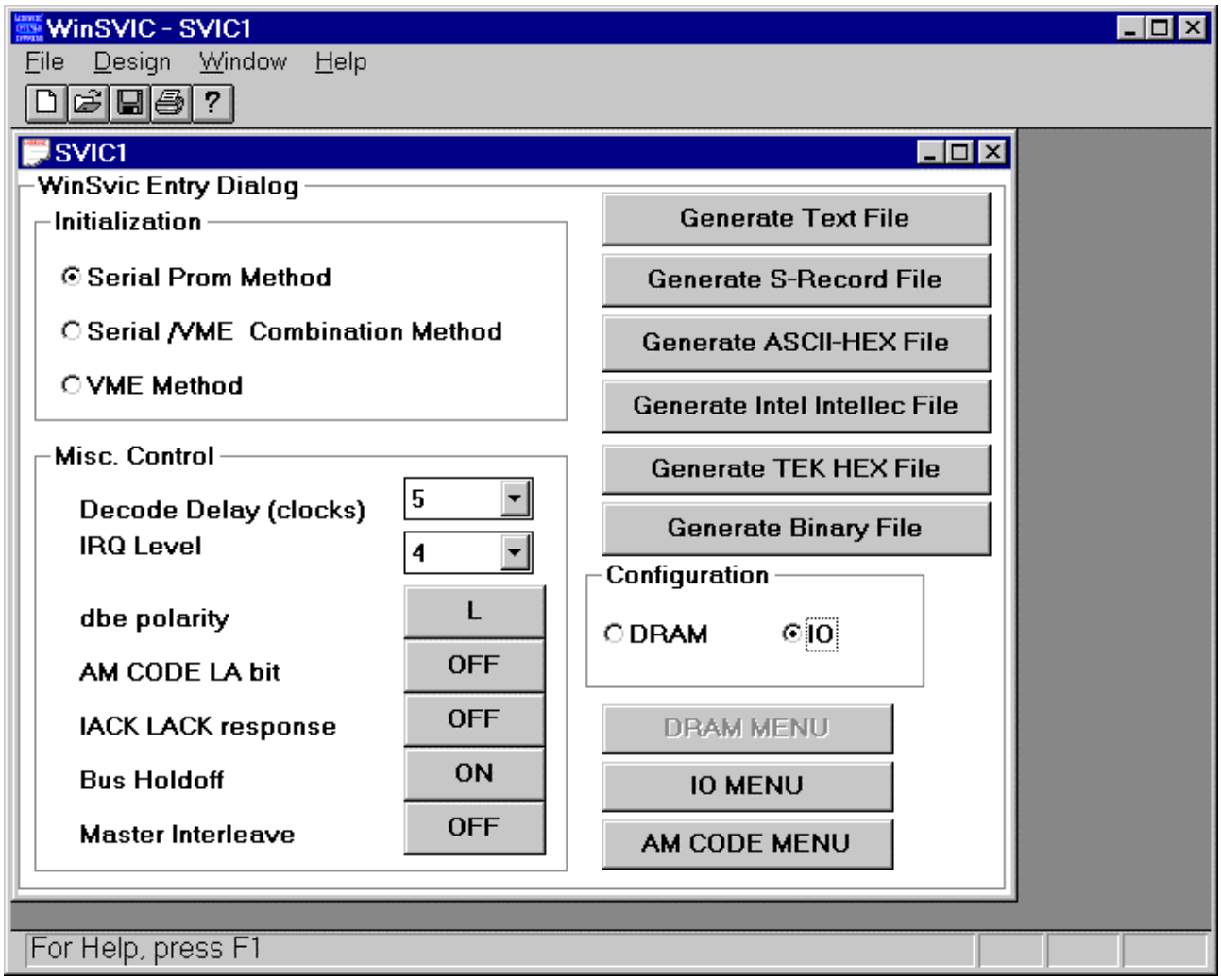
	Chip	Position
VME configuration	ATMEL AT17E65	FEA_VME_P1
VME baseaddress	AMD PALCE22V10H-7JC/5	U22
timing	AMD MACH211-7JC	U13
fpga logic (prom 0)	ATMEL 17E256	U31
fpga logic (prom 1)	ATMEL 17E256	U30
fpga statistics (prom 0)	ATMEL 17E256	U12
fpga statistics (prom 1)	ATMEL 17E256	U11

2 VME Interface

2.1 VME Interface Configuration

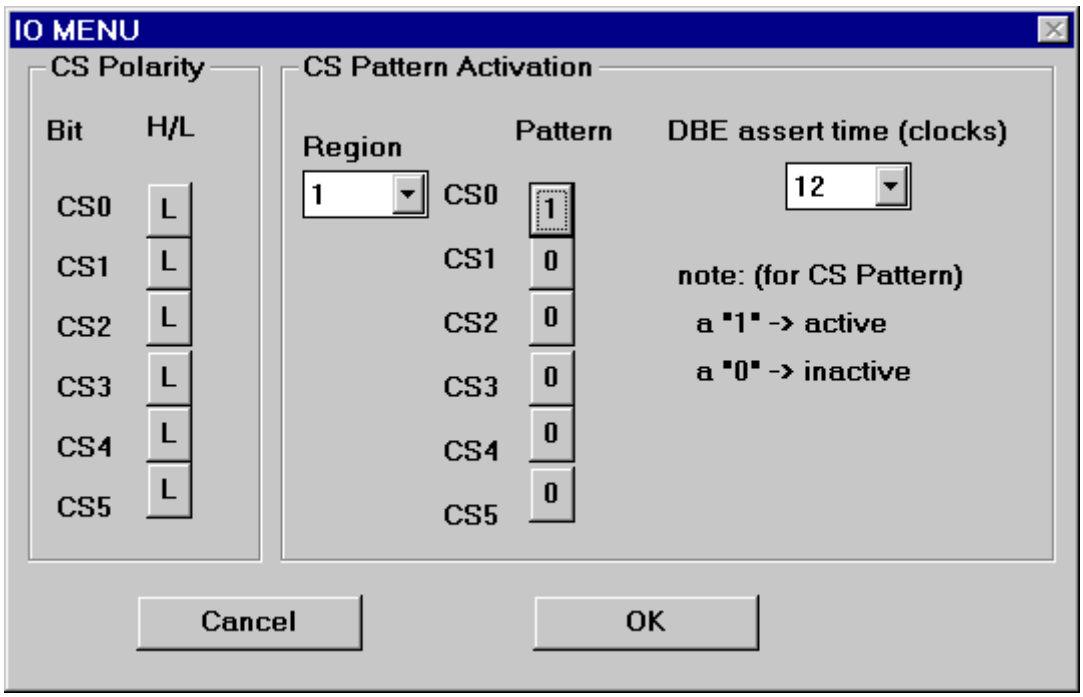
To access the VME bus the standard FEA mezzanine boards
'FEA-VME-P1' and 'FEA-VME-P2' are used. The modules have to be configured via a serial EEPROM ACTEL 'AT17E65' To generate the configuration data the program 'WinSVIC' (Cypress) has to be used.

2.1.1 Common Part



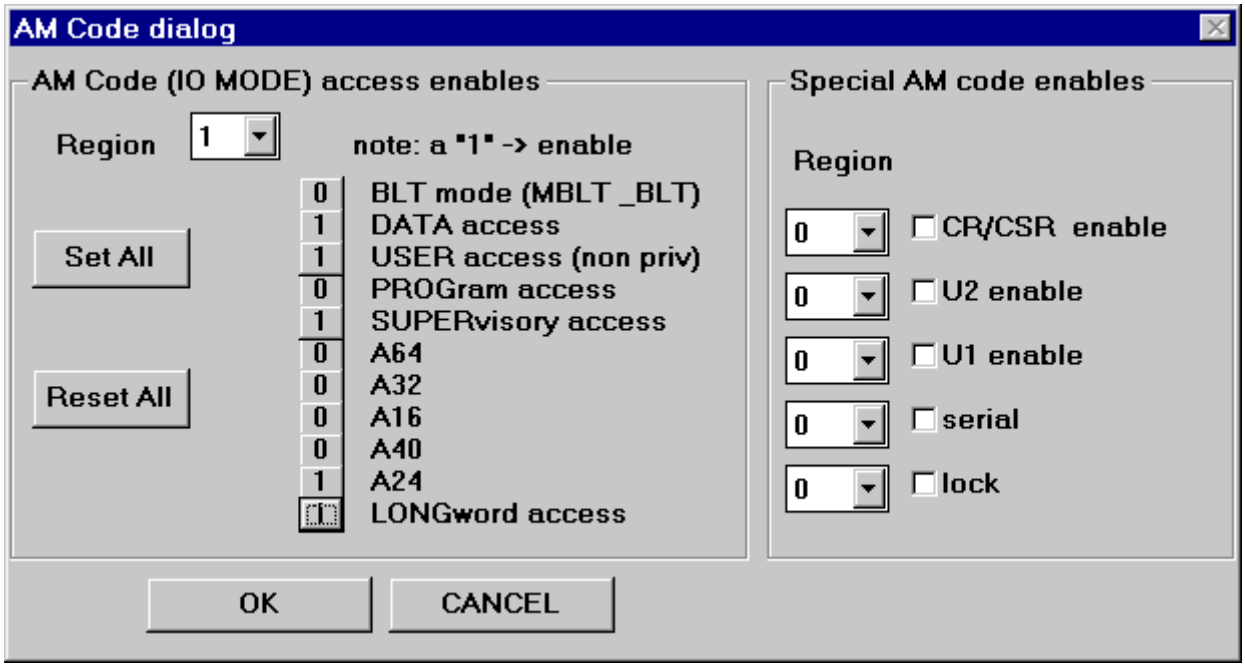
2.1.2 IO MENU Specifications

The Region 1 (input signal REG0_) is used for all VME accesses:



2.1.3 AM CODE MENU Specifications

The control command (Region 1) uses the A24 / D32 mode (AM codes '39' and '3D'):



2.2 VME Addresses

VME address (BA+...) 10 9 8 7 6 5 4 3 2	+X'..'	READ	WRITE	BITS
0 . . . 0 0 0 0 0	00	latest accept	latest accept	8
0 . . . 0 0 0 0 1	04	fifo depth	fifo depth	8
0 . . . 0 0 0 1 0	08	readout duration	readout duration	14
0 . . . 0 0 0 1 1	0C	buffer delay	buffer delay	8
0 . . . 0 0 1 0 0	10	control bits	control bits	8
0 . . . 0 0 1 0 1	14	trigger offset	trigger offset	8
0 . . . 0 0 1 1 0	18	random factor	random factor	32
0 . . . 0 0 1 1 1	1C	daughter command	daughter command	32
0 . . . 0 1 0 0 0	20	---	reset FLT counter	-
0 . . . 0 1 0 0 1	24	---	VME handshake	-
0 . . . 0 1 0 1 0	28	---	trigger at phys BX	-/8
0 . . . 0 1 0 1 1	2C	---	---	-
0 . . . 0 1 1 0 0	30	version LOGIC	---	8/-
0 . . . 0 1 1 0 1	34	---	---	-
0 . . . 0 1 1 1 0	38	---	---	-
0 . . . 0 1 1 1 1	3C	---	---	-
0 . . . 1 0 0 0 0	40	total inh cnt	reset counter	32/-
0 . . . 1 0 0 0 1	44	FP-INH inh cnt	reset SHARC link	32/-
0 . . . 1 0 0 1 0	48	VME-INH inh cnt	---	32
0 . . . 1 0 0 1 1	4C	BUF-DEL inh cnt	---	32
0 . . . 1 0 1 0 0	50	BUF-OVFL inh cnt	---	32
0 . . . 1 0 1 0 1	54	FLT-OVFL inh cnt	---	32
0 . . . 1 0 1 1 0	58	---	---	-
0 . . . 1 0 1 1 1	5C	version STAT	---	8/-
0 . . . 1 1 0 0 0	60	BX-TAG high	BX-TAG high	32
0 . . . 1 1 0 0 1	64	BX-TAG low	BX-TAG low	32
0 . . . 1 1 0 1 0	68	---	---	-
0 . . . 1 1 0 1 1	6C	---	---	-
0 . . . 1 1 1 0 0	70	---	---	-
0 . . . 1 1 1 0 1	74	---	---	-
0 . . . 1 1 1 1 0	78	---	---	-
0 . . . 1 1 1 1 1	7C	---	---	-
1 x x x x x x x x	400..7FC	histogram data	histogram data	32

BA: VME base address (bits 23...11)
‚x': used bits
‚.': don't care (not decoded)
FP-INH inh cnt: inhibited by front panel signal
VME-INH inh cnt: inhibited by VME controlled register
BUF-DEL inh cnt: inhibited by buffer delay
BUF-OVFL inh cnt: inhibited by readout buffer overflow
FLT-OVFL inh cnt: inhibited by FLT time overflow
total inh cnt: number of rejected triggers (**without** FLT time overflow inhibits)

3 Control Bits

BIT	
X'01'	Overflow Scheme
X'02'	TRIG-ENABLE (forward trigger)
X'04'	ENABLE RANDOM TRIGGER
X'08'	---
X'10'	---
X'20'	---
X'40'	---
X'80'	Readout Buffer Overflow (read only)

Overflow Scheme: **0:** use VME or LEMO handshake signal
1: use the readout duration register

4 Daughter Commands

4.1 Daughter Command Format

The 32-bit daughter command word has the following format:

31...24	23...16	15...8	7...0
COMMAND	DATA	DAUGHTER	CLUSTER

CLUSTER: cluster number (0...63), '0' means 'all clusters'
DAUGHTER: daughter number (0...63), '0' means 'all daughters of the enabled cluster(s)
DATA: command dependent data
COMMAND: daughter command code (1...7)

4.2 Command Codes

Daughter command codes and related data ('TP' = 'test pulse'):

COMMAND CODE	COMMAND	DATA
0	Latch and reset FLT count (CAN)	---
1	issue TP	TP delay(0...255)
2	load strobe pattern	strobe pattern (0...255)
3	toggle strobe	toggle pattern (0...255)
4	load BX delay	BX delay(0...255*.5ns)
5	load BX offset	BX offset (0...7)
6	load trigger mask	trigger mask (0...255)
7	load TP trigger data	TP data

trigger mask: **X'80':** hardware trigger (LEMO 4)
X'40': hardware trigger (LEMO 3)
X'20': hardware trigger (LEMO 2)
X'10': hardware trigger (LEMO 1)
X'08': TP trigger
X'04': software trigger (VME)
X'02': random trigger
X'01': FLT accept trigger

TP data: **X'80':** disable test pulse backplane
X'40': disable test pulse frontplane
X'20': enable automatic test pulse generation (at BX = 0)
X'10': --
X'08': \
X'04': \ TP Trigger BX Offset
X'02': / (0...15 * 96 ns)
X'01': /

5 SHARC-Link

For each accepted event (except for the events automatically generated by a test-pulse command) two words (48-bits each) will be sent into the SHARC-Link.

5.1 SHARC Word Format

47...44	43...40	39...36	35...32	31...28	27...24	23...20	19...16	15...12	11...8	7...4	3...0
BX-TAG											
0	0	0	TCOD	PHYS-BX		FLT-BX		FLT			

BX-TAG: BX-counter event tag
FLT: FLT-number
FLT-BX: event BX-number (from FLT)
PHYS-BX: matching physical BX-number
TCOD: trigger code

The 24 nibbles will be transferred (high-order first) with a transfer rate of 20 MHz , i.e. the total transfer time for the two words is ~ 1.2 µs.
To allow peak trigger rates the SHARC-Link transmitter logic contains a FIFO which can hold up to 16 events. If an event occurs and the FIFO is full the event will be skipped.

5.2 Trigger Codes

Trigger Code	Event Type
X'0000'	FLT-ACCEPT trigger
X'0001'	-----
X'0010'	software trigger (VME)
X'0011'	-----
X'0100'	hardware trigger (LEMO 1)
X'0101'	hardware trigger (LEMO 2)
X'0110'	hardware trigger (LEMO 3)
X'0111'	hardware trigger, not clipped (LEMO 4)
X'1000'	FLT-ACCEPT trigger + random trigger
X'1001'	random trigger
X'1010'	software trigger (VME) + random trigger
X'1011'	-----
X'1100'	hardware trigger (LEMO 1) + random trigger
X'1101'	hardware trigger (LEMO 2) + random trigger
X'1110'	hardware trigger (LEMO 3) + random trigger
X'1111'	hardware trigger (LEMO 4) + random trigger

6 Front Panel Connectors

6.1 First level Trigger Connector (FLT)

The FLT connector is a standard 2*13 pin ‚Low Profile Header' (e.g. 3M-3593-5002).
The (differential) input signals are terminated by 100 Ω resistors and received by differential line receivers AM26LS32.
The (differential) output signal is driven by a differential line driver AM26LS31.
The differential signals use positive true logic, i.e. the signal is 'true' if SIG = 'high', SIG* = 'low'.

Pin	Signal		Pin	Signal
1	GND		**2**	GND
3	BX-FLT0		**4**	BX-FLT0*
5	BX-FLT1		**6**	BX-FLT1*
7	BX-FLT2		**8**	BX-FLT2*
9	BX-FLT3		**10**	BX-FLT3*
11	BX-FLT4		**12**	BX-FLT4*
13	BX-FLT5		**14**	BX-FLT5*
15	BX-FLT6		**16**	BX-FLT6*
17	BX-FLT7		**18**	BX-FLT7*
19	GND		**20**	GND
21	FLT-ACCEPT		**22**	FLT-ACCEPT*
23	FLT-HANDSHAKE		**24**	FLT-HANDSHAKE*
25	GND		**26**	GND

6.2 SHARC Link Connector (SHA)

The SHA connector is a standard 2*7 pin ‚Low Profile Header' (e.g. 3M-3598-5002).
The (differential) output signals are driven by differential line drivers DS90C031.
The (differential) input signal is terminated by a 100 Ω resistor and received by a differential line receiver DS90C032.

Pin	Signal		Pin	Signal
1	LD2		**2**	LD2*
3	LD1		**4**	LD1*
5	LD0		**6**	LD0*
7	LD3		**8**	LD3*
9	LCLK		**10**	LCLK*
11	LACK		**12**	LACK*
13	GND		**14**	GND

6.3 LEMO Connectors

Standard LEMO connectors (DESY 26217) are being used for a few test and control signals.

6.3.1 Input Signals

The following inputs are TTL signals and terminated with 51 Ω.

BXP: Bunch crossing signal (≈ 10 Mhz)
FBXP: 'First bunch' marker (≈ 47 Khz)

The following input signals are true if low and pulled up to VCC by a 10 KΩ resistor.

TRG1: hardware trigger 1, one trigger / pulse
TRG2: hardware trigger 2, one trigger / pulse
TRG3: hardware trigger 3, one trigger / pulse
TRG4: hardware trigger 4, generates triggers as long as input is low
HSH: hardware handshake signal
FLT-DIS: disable first level trigger pulses

6.3.2 Output Signals

All output signals are available as TTL pulses (low true) and as NIM pulses.

BXP: BX-pulse
FLT-EN: FLT-ACCEPT signals are handled and forwarded
ACC: a FLT-ACCEPT signal has been accepted (pulse)
REJ: a FLT-ACCEPT signal has been rejected (pulse)
HSH: a handshake signal has been received (hardware or software)

6.4 Backplane Connector (P2)

The Non-VME-Standard part of P2 (rows ‘a’ and ‘c’) is being used for distribution of the fiber link data to the fiber link transmitter modules.
The unipolar signals are driven by bus drivers 74ABT574, the differential signal is driven by a differential line driver DS90C031.

	a	c
1	FIBER0	FIBER1
2	FIBER2	FIBER3
3	FIBER4	FIBER5
4	FIBER6	FIBER7
5	FIBER8	FIBER9
6	FIBER10	FIBER11
7	FIBER12	FIBER13
8	FIBER14	FIBER15
9	FIBER16	FIBER17
10	FIBER18	FIBER19
11		
12	GND	
13		
14		
15		
16		
17	BX-PULSE (a)	BX-PULSE (a)*
18	BX-PULSE (b)	BX-PULSE (b)*
19	BX-PULSE (c)	BX-PULSE (c)*
20	BX-PULSE (d)	BX-PULSE (d)*
21	BX-PULSE (e)	BX-PULSE (e)*
22	BX-PULSE (f)	BX-PULSE (f)*
23	BX-PULSE (g)	BX-PULSE (g)*
24	BX-PULSE (h)	BX-PULSE (h)*
25		
26		
27		
28		
29		
30		
31		
32		

6.4.1 Fiber Link Data Word

The 20-bit fiber link data words have the following format:

	19 ... 16	15 ... 8	7 ... 0
FLT EVENT	1 0 0 0	0 0 0 0 0 0 0 0	FLT-BX #
RANDOM TRG	1 0 0 1	0 0 0 0 0 0 0 0	FLT-BX #
VME TRG	1 0 1 0	0 0 0 0 0 0 0 0	FLT-BX #
LEMO1 TRG	1 1 0 0	0 0 0 0 0 0 0 0	FLT-BX #
LEMO2 TRG	1 1 0 1	0 0 0 0 0 0 0 0	FLT-BX #
LEMO3 TRG	1 1 1 0	0 0 0 0 0 0 0 0	FLT-BX #
LEMO4 TRG	1 1 1 1	0 0 0 0 0 0 0 0	FLT-BX #
COMMAND HIGH	0 1 1 0	0 0 0 0 0 A A A	DATA
COMMAND LOW	0 1 1 1	0 0 D D D D D D	0 0 C C C C C C
FLT #	0 1 0 1	FLT #	
BX #	0 0 0 0	0 0 0 0 0 0 0 0	BX #

A: command code
D: daughter number
C: cluster number

7 Revision History

- **10-Jun-98:** Revision 3
- **05-Aug-98:** Version control for XILINX chips added ('LOGIC', 'STATISTICS'), -> **version 1**
- **19-Aug-98:** 'CLR_FLT' and 'VME_HSH' pulse generation changed ('LOGIC')
- **19-Aug-98:** VME trigger logic changed (ignore trigger offset), -> **'LOGIC' version 2**
- **14-Sep-98:** Trigger mask description corrected (in manual)
- **19-Sep-98:** Daughter command timing changed, -> **'LOGIC' version 3**
- **10-Oct-98:** SHARC link algorithm changed, -> **'STATISTICS' version 2**
- **22-Oct-98:** FLT number generation (SHARC link) corrected, -> **'STATISTICS' version 3**
- **08-Dec-98:** READOUT DURATION register changed to 9 bits
- **08-Dec-98:** FLT-BX number handling corrected
- **08-Dec-98:** Trigger codes (SHARC link) changed, -> **'LOGIC' version 4**
- **12-Jan-99:** Readout Buffer Overflow generation corrected, -> **'LOGIC' version 5**
- **28-Jan-99:** Statistics and Histogram Timing changed, -> **'LOGIC' version 6**
- **28-Jan-99:** Statistics and Histogram Timing changed, -> **'STATISTICS' version 4**
- **23-Apr-99:** Synchronization of 'FLT_DIS' signal (LEMO) added, -> **'LOGIC' version 7**
- **08-Jun-99:** Automatic test pulse generation feature added (in manual)
- **05-Apr-00:** READOUT DURATION register changed to 14 bits, ->**'LOGIC' version 8**
- **27-Jun-00:** Hardware Trigger 4 generates triggers as long as input is low, ->**'LOGIC' version 9**